Index

A, B
architecture, 131-133
bin packing problem, 154

C
chromatic number, 29, 32-35
code rewriting technique, 9
computer assisted design software, x
conflict (open/closed/cost), 29, 32
CPU time, 49, 77, 97, 105-108, 124, 128, 153

D
data assignment-data structure-data storage-data transfer, 8-21
data binding, 16-21

E
electronic chip design process, 54
electronic design, 11-25
embedded system, 2-4
external memory, 19-21

F, H
Friedman test, 105, 106, 128
hardware, 11-16

I
ILP formulation, 31-32, 61-63, 80-84, 113-116
in-place mapping optimization, 13
initial solution, 86-89
iterative metaheuristic approach, 119-123

K, L
k-weighted graph coloring problem, 57, 63, 65, 73, 75, 83, 96, 148
localsolver, 73, 96, 124, 125, 128
M
mapping, 13, 14
MemExplorer, 131-144
memory conflict graph (MCG), 131, 143-139
memory management-
memory allocation
problem-memory bank,
memory architecture-
memory partitioning, 1-25

N, O
neighborhood, 91-93
on-chip memory bank capacity, 132
optimization technique,
8-21

P
parsing yield, 133
power consumption, 4-8

R, S, T
register allocation, 15
scratchpad memory (SPM), 14
software, 9-11
tabu search procedure,
66-69, 89-91

V
variable neighborhood search (VNS), 19, 77, 3-94
vertex coloring problem, 12

power performance, 4-8
proposal metaheuristic,
65-71, 85-94