1.1. Introduction

Power dissipation in switching devices is considered today as the most important roadblock for future nanoelectronic circuits and systems [SAK 04]. The complementary metal-oxide-semiconductor (CMOS) power consumption consists of two contributions: the dynamic and the static leakage components. In the past, the power increase was due to the different scaling factors for the voltage supply and the device geometry being essentially dominated by the dynamic power. Added to the dynamic power, there is an additional power component, the subthreshold leakage, which starts to dominate for advanced technology nodes and practically limits the supply voltage of modern integrated chip (IC) to a lower limit of 0.5 V. As the technology nodes scale, we have to use a lower supply voltage and, as the threshold voltages are reduced, the leakage or off current, \(I_{\text{off}}\), becomes dominant because the subthreshold swing, \(S\), of a metal-oxide-semiconductor field-effect transistor (MOSFET) is unscaleable and tied to the thermal value of 60 mV/decade at room temperature [GOP 05]. This refers to the gate voltage required to change the drain current by one order of magnitude when the transistor is operated in subthreshold and is defined by

\[
\text{SS} = \frac{\partial V_g}{\partial (\log I_d)} = \frac{\partial V_s}{\partial \psi_s} \frac{\partial \psi_s}{\partial (\log I_d)} = \left(1 + \frac{C_d}{C_{\text{ox}}} \right) \frac{kT}{q} \ln 10 \quad [1.1]
\]

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where $\Psi_S$ is the surface potential, $V_g$ is the gate voltage, $kT/q$ is the thermal voltage and $C_d$ and $C_{ox}$ are the depletion and the oxide capacitance, respectively. The subthreshold leakage problem cannot be solved by any advanced engineering if we rely on the MOSFET principle. Various device solutions have been proposed to reduce the $m$ and $n$ factors of equation [1.1] below their fundamental thermal limits of 1 and $\ln(10) kT/q$, respectively. Here, subthermal is what we call the values of the subthreshold swing less than $kT/q \ln(10)$ (e.g. less than 60 mV/dec at room temperature, $T = 300$ K). A subthermal subthreshold swing by reducing the $n$ factor involves the modification of the conduction or carrier injection mechanism; impact ionization [CHE 08] and quantum mechanical band-to-band tunneling (BTBT) mechanism have been proposed [BOU 09a, QUI 78] as major solutions. Recently, tunnel field effect transistor (FETs) [QUI 78, BAN 87, TAK 88, BAB 92] exploiting BTBT have emerged as candidates for ultralow standby power switches. However, one major drawback of tunnel FETs is their intrinsically low on-current capability, which is in best case one-to-two order of magnitude less compared to silicon nano-CMOS.

Another solution to lower $S$ is to reduce below 1 the body factor, $m$, in equation [1.1]. This can be achieved by using the recently proposed negative capacitance effect [RED 95, KOG 96, HAN 00] or by using electromechanical gates [AYD 04] (with a movable electrode) where instability points between electrical and mechanical forces are used to define infinitely abrupt transitions between off and on states in micro/nanoelectromechanical (M/NEM) relays.

1.2. Tunnel FETs

Compared to other steep slope devices, tunnel FETs seem today the most promising abrupt switches; they do not suffer from the reliability problems such as the impact ionization abrupt switches, I-MOS and the nanoelectromechanical (NEM) relays. Moreover, in both I-MOS and NEM relay, the voltage scaling below 1 V is extremely challenging, being limited not only by the device engineering but also by their fundamental physics.

The basic design of tunnel FET is a gated p-i-n diode where the band-to-band tunneling takes place between the intrinsic and p+ regions, for n-type
devices (see Figure 1.1). To operate tunnel FET devices, the p-i-n diode is reverse-biased (for the energy band simulations reported in Figure 1.1, the source is grounded and positive voltages are applied to the drain and to the gate). With a zero gate voltage, the width of the energy barrier between the intrinsic region and the p+ region is wide (larger than 10 nm, one approximate minimum usually adopted for defining the limit of a significant tunneling probability), and the device is in the OFF-state. As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow.

![Figure 1.1. Principle of tunnel FET and corresponding energy band diagrams in OFF and ON states with their control by the gate voltage](image)

The tunnel MOSFET offers an appealing concept for a substantial lowering of the energy dissipated in a switching device by replacing the thermionic emission of charge carriers over a barrier to enter the MOSFET channel with a tunneling process. If the tunneling process is made sufficiently effective, tunnel FETs can ultimately yield an effective cooling of the injecting source contact through a band-pass filter action that enables steep inverse subthreshold slopes over many orders of magnitude, thus providing low values of the average subthreshold swing, SS_{avg}.

Some of the first-tunnel FETs were proposed in 1978 followed by a small number of subsequent publications dealing with silicon and III–V surface tunnel transistors. Since approximately 2000, the field has been rapidly
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Evolving and, recently, tunnel FETs have attracted an increasing amount of interest due to their potential ability to enable switching with an inverse subthreshold slope steeper than 60 mV/dec. The following list of categories shows the most important contributions to the field and the present state-of-the-art of tunnel FETs.

First, realizations of interband tunneling transistors.— Quinn et al. at Brown University [QUI 78], were the first to propose the gated p-i-n structure of a Tunnel FET in 1978, and suggested the usefulness of this device for spectroscopy. Banerjee et al. [BAN 87] studied the behavior of a three-terminal silicon tunnel device, and Takeda et al. [TAK 88] showed the lack of VT roll-off when scaling. Baba fabricated tunnel FETs, which he called surface tunnel transistors in III–V materials [BAB 92]. In 1995, Reddick and Amaratunga published measured characteristics of silicon surface tunnel transistors [RED 95]. In 1997, Koga and Toriumi proposed a post-CMOS three-terminal forward-biased silicon tunneling device [KOG 96]. In 2000, Hansch et al. reported experimental results from a reverse-biased vertical silicon tunneling transistor made with MBE with a highly-doped boron delta-layer and noted the saturation behavior in the ID-VG characteristics [HAN 00]. Aydin et al. fabricated Lateral Interband Tunneling Transistors on silicon-on-insulator (SOI) in 2004 [AYD 04]. These devices were like tunnel FETs with no intrinsic region and the gate over a p-n junction, aiming to reduce gate capacitance and therefore increase speed. As a particular feature, the authors claim that there should be no current saturation for these devices.

Tunnel FETs in the Si/SiGe material system.— In 2004, Bhuwalka et al. published the first of many articles about their vertical tunnel FET on silicon with a SiGe delta layer, grown by MBE [BHU 04]. The SiGe replaced the silicon delta layer already used by Hansch, and, in theory, the smaller bandgap reduces the tunnel barrier width and increases tunneling current in the on-state as well as lowering the subthreshold swing. In 2006, the same group proposed a lateral tunnel FET on SiGe-on-insulator, and showed through simulation that on-current would increase with the percentage of Ge in the SiGe [BHU 06].

In 2007, Boucart and Ionescu showed the first comprehensive numerical simulations of Si tunnel FETs with a high-\(k\) gate dielectric and double-gate structure [BOU 07a]. The better capacitive control of the tunnel junction improves both the on-current and the subthreshold swing. The same authors
also presented a method of threshold voltage extraction for tunnel FETs that has a physical basis (related to the saturation of the energy tunneling barrier), demonstrated a second threshold voltage in relation to the drain [BOU 07b], and showed that tunnel FETs have the potential for high gain at low applied voltages. The second threshold voltage was shown to be caused by drain-induced-barrier-thinning due to the p-i-n structure of tunnel FETs.

In 2008, Nayfeh et al. simulated and measured tunnel FETs with a strained SiGe channel layer and the drain on the n-type silicon substrate. Significantly improved device characteristics were obtained with increasing Ge content [NAY 09]. Also, in 2008, first experimental tunnel FETs in strained Ge [KRI 08] were demonstrated by Krishnamohan et al. that exhibited a point slope, i.e. an inverse subthreshold slope in a small-gate voltage range, of 50 mV/dec. In addition, Mayer et al. from CEA-LETI showed experimental results for silicon-, germanium- and SiGe-on-insulator and demonstrated an inverse subthreshold slope of 42 mV/dec in ultrathin body (UTB) SOI tunnel FETs for p-channel operation (Figure 1.2(a)) [MAY 08]. Using silicon-germanium on insulator (SGOI) and GOI TFETs, strong improvements of the driving current, between several hundreds and thousands, are obtained compared with SOI transistors (Figure 1.2(b)). \(I_{off}\) is very low but \(I_{on}\) is only of the order of several \(\mu A/\mu m\) for the best GOI TFETs [MAY 08].

Verhulst, et al. at IMEC studied the optimization of nanowire tunnel FETs by changing the source material to Ge [VER 08a]. The band discontinuity between Si and Ge leads to a significantly enlarged BTBT probability.

Boucart et al. from Ecole Polytechnique Fédérale de Lausanne (EPFL), in Switzerland, proposed a silicon-only tunnel FET with a lateral strain profile to decrease the bandgap at the tunnel junction and therefore improve device characteristics [BOU 09b]. Moselund et al. from IBM Zurich presented tunnel FETs on \textit{in-situ} doped VLS grown silicon nanowires with different gate dielectric material [MOS 09]. Fully-depleted Ge tunnel FETs were investigated by Zhang et al., first using simulations [ZHA 09]. More recently, experimental demonstrations of a heterostructure design for tunnel field effect transistors with two low-direct bandgap group IV compounds, GeSn and highly tensely strained Ge in combination with ternary SiGeSn alloy by Wirths et al., have pushed forward the performance of these devices [WIR 13].
**III–V and III–V hetero-junction tunnel FETs.**—There are basically two different approaches for III/V based devices. The first approach is similar to the SiGe tunnel FETs, where the source consists of an SiGe alloy to decrease the effective bandgap and provide higher on-currents compared to an all-silicon tunnel FET. However, an SiGe-based source is only a solution for the n-type tunnel FET as pointed out by Verhulst et al [VER 08b]. For a p-type tunnel FET a device with III/V source was proposed enabling the realization of inverters etc. Suitable materials for such p-type tunnel FETs are, for instance, InAs and InxGa1-xAs, where the latter would be easier to fabricate due to the smaller lattice mismatch. InAs, having a smaller bandgap, would on the other hand bring higher on-currents. The main advantage of this type of tunnel FET is that both polarities can be implemented on silicon and would be CMOS compatible.
Several groups have investigated all III/V tunnel FETs by simulation in two main configurations. The simplest structure consists of a p-i-n structure in the same III/V material such as InAs [MOO 08, ZHA 08, LUI 09]. If doping profiles can be controlled, the authors report a better performance than both Si- and Ge-based tunnel FETs at low supply voltages (<0.5 V). Furthermore, both Ge and InAs based tunnel FETs show clear advantages in energy-delay-product and switching delay as VDD is scaled toward 0.25 V.

In 2009, Knoch investigated the use of III–V heterojunctions for tunnel FETs since they offer the possibility of studying the impact of staggered to broken band line-ups [KNO 09]. It was found that a broken band line-up yields an inverse subthreshold slope close to 60 mV/dec and a staggered line-up is beneficial for steep slope III–V devices.

For very short gate lengths Gate-All-Around InAs TFETs, small wire diameters are needed, down to 5 nm or below, in order to obtain a good subthreshold swing (Figure 1.3) [CON 11].

![Figure 1.3. Subthreshold swing versus gate length for GAA InAs nanowire TFETs for various wire diameters obtained by quantum simulation](image)

High performances, with $I_{on}$ up to 1 mA/µm at low $V_d$, have been demonstrated by quantum transport simulation on strained InAs NW TFET (Figure 1.4), the best result being shown for a biaxial strain [CON 11].
However, the on-current improvements can be frustrated by the degradation of the swing in the presence of traps. Both traps and surface roughness can also be a relevant source of device variability for tunnel FETs [CON 12].

**Tunnel FETs based on alternative materials.**— The bandgap engineering exploiting other 1D and 2D materials attracted interest for alternative implementations of tunnel FETs. Employing a dual-gate carbon nanotube tunnel FET Appenzeller et al. demonstrated BTBT with an $S = 40 \text{ mV/dec}$ [APP 04]. The same group showed in another work, that in an optimized carbon nanotube tunnel FETs an $S = 10 \text{ mV/dec}$ would be possible [APP 05]. In 2006, Zhang from Stanford demonstrated an experimental carbon nanotube p-i-n tunnel transistor exhibiting a minimum inverse subthreshold slope of 25 mV/dec [ZHA 06]. In 2009, Koswatta et al. at Purdue University showed a comparison of tunnel FET and MOSFET performance, based on devices built on carbon nanotubes [KOS 09]. Poli et al. studied the ultimate scaling limits of carbon nanotube tunnel FETs [POL 08].

A comprehensive review of fabricated tunnel FETs and their experimental characteristics has been proposed by Seabaugh [SEA 10], concluding that their main promise is in their ability to provide higher drive

![Figure 1.4. 20 nm gate length InAs NW TFET with 5 nm diameter and different strains obtained by quantum simulations](image)

\[ V_{ds} = 0.3 \text{ V} \quad L_g = 20 \text{ nm} \]
current than the MOSFET as supply voltages approach 0.1 V. His overview of experimental characteristics for p- and n-type tunnel FETs are reproduced in Figures 1.5(a) and (b), which also compared tunnel FETs with I-MOS switches. It has been concluded that a lot of progress in provided high on currents and steep subthreshold swings over many decades is still expected.

In addition to logic circuits, the application of TFETs in static random access memory (SRAM) has been reported [CHE 13]. SRAMs designs with CMOS and TFET technology using different transistor numbers (6T, 7T and 8T) were compared in terms of switching behavior, output characteristics and stability. An improvement of 700-fold leakage reduction was demonstrated using TFET over CMOS technology in silicon TFET SRAM [SIN 10].

Further attractive applications of TFETs are in analog integrated circuits such as ultralow-power voltage controlled oscillators or voltage references [MAL 12, FUL 08].

![Figure 1.5. Experimental Tunnel FET characteristics for a) p-type and b) n-type, as collected by Seabaugh [SEA 10] and their comparison with data on I-MOS switches (©2010 IEEE). For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip](image)
1.3. Ferroelectric gate FET

Exploiting the ferroelectric polarization in the gate stack to control the inversion charge of a FET channel provides a uniquely compact one-transistor device with an active gate stack; to date many studies have been reported concerning memory applications. Sallahuddin et al. [SAL 08a] have proposed using ferroelectrics in order to exploit their unique nonlinear energy dependence on polarization to provide a negative capacitance effect. However, the difficulty in demonstrating the principle of negative capacitance experimentally is related to the fact that the exploited instability should be controlled (stabilized) by an in-series positive capacitance and, for defining an abrupt transition from off-to-on state, place the stabilized negative capacitance region in the subthreshold operation of the MOSFETs. First attempts to experimentally demonstrate such a ferroelectric abrupt switch (Fe-FET) were reported by Salvatore et al. [SAL 08b] and Rusu et al. [RUS 10]; the last report in particular can by far be considered the first experimental result of a sub-thermal swing at room temperature. A key advantage of the Fe-FET is that, in contrast to tunnel FETs, its on-current is as high as the one of a conventional MOSFET. In this chapter, we focus on the characteristics of metal-ferroelectric-metal-oxide-semiconductor structures recently reported by the EPFL group [SAL 08b, RUS 10] based on a complete set of experiments exploiting the internal metal contact.

Figure 1.6(a) depicts a three-dimensional (3D) view of the Fe-FET under investigation, exhibiting such a negative capacitance effect: it consists of a conventional silicon p-type MOSFET (made in a n-type well laterally isolated by Shallow-Trench-Isolation (STI) filled with silicon dioxide to minimize the leakage sources), with a 50 nm layer of P(VDF-TrFE) (70–30%) ferroelectric copolymer integrated in the gate stack. The poly(vinylidene fluoride/trifluoroethylene), P(VDF-TrFE), is a wide-bandgap semicrystalline polymer that was selected for our investigations because of its low temperature processing (annealing temperature less than 180°C), possibility to spin-coat very thin film on full wafers, low-leakage current and excellent ferroelectric properties in sub-100 nm layers [NAB 05]. At a VDF:TrFE ratio of about 70:30, this copolymer is ferroelectric [BRA 06] A particularity of this device is the 50 nm thin metal layer (AlSi) sandwiched between the ferroelectric and SiO$_2$, with a double

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role: (1) to act as a floating equipotential metal plane between the ferroelectric and the intrinsic MOS transistor gate and exploit in such a structure the negative susceptibility of multi-domain films governed by the electrostatic according to previous results of Bratkovsky [BRA 06] concerning ferroelectrics sandwiched between metal electrodes and, (2) to enable direct measurements on the internal voltage potential, $V_{\text{int}}$, by probing the potential of the internal metal layer with a high-impedance voltmeter (therefore investigate ferroelectric polarization in all regimes of operation).

From equation [1.1], the device design condition for achieving a sub-thermal swing is expressed in terms of the amplification of the surface potential, $d\Psi_S/dV_g$, or in terms of the body factor, $m$

$$0 < m = \left[ \frac{d\Psi_S}{dV_g} \right]^{-1} = \left[ \frac{d\Psi_S}{dV_{\text{int}}} \right]^{-1} = \frac{1}{G} \left[ \frac{d\Psi_S}{dV_{\text{int}}} \right]^{-1}$$

where $G = dV_{\text{int}}/dV_g$ is the internal voltage gain, directly accessible by measurement in our Fe-FET structure with internal metal contact. If the ferroelectric capacitance is assumed negative, $C_{\text{ferro}} < 0$, and with $V_{\text{ferro}} = V_g - V_{\text{int}}$ the key design conditions for sub-thermal subthreshold swing due to a stabilized negative capacitance by in series $C_{\text{ox}}$ and $C_d$, are

$$C_{\text{MOS}} = \frac{C_{\text{ox}}C_d(V_{\text{int}})}{C_{\text{ox}} + C_d(V_{\text{int}})} < -C_{\text{ferro}}(V_{\text{ferro}}) < C_{\text{ox}}$$

Conditions [1.3] are difficult to simultaneously fulfill in practice because of the dependence of both $C_d$ and $C_{\text{ferro}}$ on the internal voltages and, for our device, also because of the process variability of the ferroelectric thickness. Fulfilling the conditions [1.3] in a limited range of gate voltage (subthreshold) operations of the Fe-FET results in hysteretic $I_d-V_g$ characteristics with sub-thermal transitions limited to the regions where the internal voltage gain is achieved.

The negative capacitance condition can be written as function of the polarization, $P$, and the gain, $G$
Therefore, an internal voltage amplification, $G > 1$, is directly linked to the existence of the negative capacitance effect, Figure 1.6(b).

Figure 1.6(c) shows a high-resolution TEM of the fabricated Au/P(VDF-TrFe)/AlSi/SiO$_2$ gate stack. Figure 1.6(d) is an AFM image of the deposited polymer layer showing a variability of the P(VDF-TrFE) topography in the order of 20 nm and an average thickness of 50 nm. The Fe-FETs reported here, have been designed so that their $C_{ox}$, $C_{ferro}$ and $C_{MOS}$ could verify conditions [1.3].

$$C_{ferro} = \frac{dP}{dV_{ferro}} = \frac{dP}{d(V_g - V_{int})} = \frac{dP}{dV_{int}} \frac{G}{1 - G} < 0$$ [1.4]

**Figure 1.6.** a) Cross-section of the fabricated p-type metal-ferroelectric-metal-oxide semiconductor field effect transistor with internal gate contact, $V_{int}$, within an n-well and with STI isolation. b) Qualitative depiction of the conditions to be fulfilled by the gate stack capacitances for a sub-thermal subthreshold swing: CMOS $< -C_{ferro} < C_{ox}$ and illustration of the capacitive divider of the gate stack. c) TEM cross sectional image of the fabricated device: 1 = silicon substrate, 2 = silicon dioxide, 3 = aluminum, 4 = PVDF-TrFE, 5 = gold. The thickness variability of the PVDF-TrFe layer is clearly visible. d) AFM topography of the ferroelectric layer: the average thickness is ~50 nm while the variability is in the order of 20 nm. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip
Figure 1.7(a) reports the $I_d-V_g$ characteristics of the intrinsic MOSFET (with the gate bias directly applied on the internal contact, $V_{\text{int}}$) and the Fe-FET (with the gate bias applied on the top Au contact, $V_g$, and with the internal contact being left floating). As expected, the ferroelectric induces a voltage-controlled hysteresis in the current–voltage characteristics. Surprisingly, even if equivalent-oxide-thickness (EOT) of the Fe-FET using the full gate stack is significantly larger, the subthreshold swings in the “up” and “down” directions (indicated by arrows in Figure 1.7(a)) are not degraded in Figure 1.7(b). We observe that in the “down” direction, the swing of the Fe-FET is at the thermal limit of 60 mV/decade (this is the lowest ever reported/achieved thermal swing in a bulk silicon FET). Figure 1.7(c) reports the butterfly $C-V$ characteristics, which are the typical signature of a ferroelectric gate stack, compared to the non-hysteretic quasi-static $C-V$ characteristics of the internal transistor (using only SiO$_2$ as gate dielectric) measured on the same Fe-FET device. This figure shows an excellent correlation between the regions where the minimum of the subthreshold swings is observed and the low values of the gate stack capacitance, where the negative capacitance is fulfilled. Despite the noisy quasi-static $C-V$, in systematic experiments we observe some reversed peaks or locally flat values of the capacitance.

Figure 1.8 reports the unique experimental investigation enabled by the internal metal contact: the characteristics of the Fe-FET are measured while the $V_{\text{int}}$ contact is probed with a high-impedance voltmeter configuration. A typical hysteretic dependence $V_{\text{int}}-V_g$ is reported in Figure 1.8(a). Figure 1.8(b) shows that the highest peaks of the internal voltage gain, $G = dV_{\text{int}}/dV_g > 1$ are perfectly correlated with the minimum swing, which is lower compared to that of the intrinsic transistor (~80 mV/dec).

This is clear proof of the negative capacitance effect. The $V_{\text{int}}-V_g$ plot permits the extraction of the ferroelectric polarization loop, $P$, versus the voltage drop on the ferroelectric, $V_{\text{ferro}}$, based on the following simple relation derived by the application of the Gauss law at the ferroelectric-SiO$_2$ interface

$$P = \left[ \frac{(V_{\text{int}} - \Psi_S)k_{\text{ox}}}{t_{\text{ox}}} - \frac{V_g - V_{\text{int}}}{t_{\text{Fe}}} \right] \times \epsilon_0$$  \[1.5\]

where $\Psi_S$ is the MOSFET surface potential, $k_{\text{ox}}$ is the relative permittivity of the SiO$_2$, $\epsilon_0$ is the vacuum permittivity, and $t_{\text{ox}}$ and $t_{\text{Fe}}$ are the thicknesses of
oxide and ferroelectric layers, respectively. The surface potential $\Psi_s(V_{\text{int}})$ is calculated according to the full-analytical equation of a conventional MOSFET\textsuperscript{11} from depletion to strong inversion. Figure 1.8(c) reports the resulting experimental minor loops, $P-V_{\text{ferro}}$.

![Figure 1.7](image-url)

**Figure 1.7.** a) Drain current, $I_d$, versus gate voltage, $V_g$, characteristics of the Fe-FET (hysteretic) with metal-ferroelectric-metal-SiO$_2$ gate stack and of the internal MOSFET (non-hysteretic) using SiO$_2$ as gate dielectric, for $V_d = 50$ mV. The channel dimensions are: length $= 50$ $\mu$m and width $= 20$ $\mu$m. b) Calculated point subthreshold swings, SS, of the Fe-FET based on experimental data c) Quasi-static capacitances of the internal MOSFET, $C_{\text{int}}$, (circles) and of the ferroelectric gate stack, $C_{\text{ferro}}$ (squares) measured on the same device. All the measurements are performed with the internal metal contact floating (not connected). For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip
Figure 1.8. a) Drain current versus gate voltage experiment and corresponding hysteretic internal voltage, Vint, (inset: experimental setup for test conditions, with internal contact connected to a high impedance voltmeter). The hysteretic Vint has a change of slope in the off to on transitions (weak inversion) of the Fe-FET. b) Corresponding subthreshold swings (squares), SS, and internal voltage gain (circles), dVint/dVg. The region of highest internal voltage gain peaks (dVint/dVg ~1.1) corresponds to the lowest SS ~72 mV/decade. Note that when probing the internal contact the Fe-FET subthreshold swing is slightly degraded compared with the case when Vint is left floating and the characteristics shifted to the right (as showed in the supplementary material). c) Polarization versus ferroelectric voltage minor loops showing a clear S-shape region in the voltage range where the internal voltage gain is maximum. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip
Another experimental proof of the negative capacitance is the S-shape of $P-V_{\text{ferro}}$ or the negative slope of the polarization versus voltage drop on the ferroelectric layer ($dP/dV_{\text{ferro}} < 0$) that confirms equation [1.5]. The inset of Figure 1.8(c) clearly demonstrates that such a region is achieved in the Fe-FET device in the sweep-down of the $V_g$ (corresponding to the region where SS is lowered compared to the reference transistor). As the minor loop is not symmetrical, a similar condition is not achieved in the sweep-up of the $V_g$ for the same device. In the corresponding S-shape region, $G$ value is maximal (peak) and larger than 1. Due to the non-uniformity of PVDF-TrFe layer, the negative capacitance condition is not identically achieved in all the devices.

An important property of negative capacitance in Fe-FET concerns the influence of the temperature of the internal voltage amplification, $G$, and the S-shape region of ferroelectric polarization that is requirement for sub-thermal subthreshold swings. According to the Landau–Devonshire theory of ferroelectrics [TAG03, GIN01], the Helmholtz free energy, $F$, can be truncated with respect to the macroscopic polarization, $P$ according to

$$ F = \frac{1}{2} \alpha(T)P^2 + \frac{1}{4} \beta P^4 + \frac{1}{6} \gamma P^6 - EP \quad [1.6] $$

where $E$ is the electric field and $\alpha$ coefficient is a linear function of temperature, vanishing at the Curie temperature $T_0$

$$ \alpha = \frac{1}{\varepsilon_0} \frac{T-T_0}{C_{CW}} \quad [1.7] $$

where $C_{CW}$ denoting the Curie–Weiss constant. Parameters $\beta$ and $\gamma$ are independent of the temperature. Note that $\alpha$ is positive in the paraelectric phase and negative in the ferroelectric phase.

Figure 1.9 qualitatively shows that only below the Curie temperature ($T < T_0$), when the first term of expression [1.6] is non-zero, does the free energy have a local maximum that conditions the negative capacitance effect. When approaching $T_0$, the $P^2$ term of expression [1.6] is reduced and the negative capacitance effect weakens and eventually disappears at $T_0$, as the unstable equilibrium region in the energy–charge dependence (local maximum) will disappear [SAL10]. The corresponding slope of electric field versus polarization, $dE/dP$ is negative (S-shape) in the region of
negative capacitance for $T < T_0$ and when the $P^2$ term cancels out in equation [1.6], $\frac{dE}{dP}$ becomes positive for $T > T_0$.

\[ \text{Figure 1.9. a) Effect of temperature on the Helmholtz free energy, } F. \text{ b) Effect of temperature on the S-shape } P-E \text{ characteristics. } T_0 \text{ is the Curie temperature: for } T < T_0 \text{ the material is in the ferroelectric phase. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices2.zip} \]

In summary, the polarization S-shape, and therefore, the negative capacitance effect, could vanish by increasing the temperature while the capacitance of the ferroelectric gate stack increases, in agreement with Laudau–Devonshire theory of ferroelectrics. This means that any practical negative ferroelectric gate stack should be designed with a Curie temperature higher than the device operation point in integrated circuits ($>100^\circ$C).

1.4. Bibliography


