Index

Adaptive algorithm
communication link, 251
fault currents, 251–252
flow chart, 251, 253
recloser operating time, 252, 255, 256
TCC, 252, 254

Band-NV strategy
algorithm
flowchart, 88, 89
implementation, 90
NP voltage variation, 88, 90
pseudocode, 88, 90
controllable intervals, 84
conventional criterion, 83–84
DC-link capacitors, 83
effective switching frequency, 93–94
locally averaged NP current, 83
NP reference voltage, 85
NP voltage ripple, 91–93
operating regions
CIs and UIs, 85
fundamental cycle, 85, 86
modified band criterion, 87
NPC converter, 85, 87
peak–peak NP voltage ripple, 85
simulation results
duty cycles, 99
fundamental cycle, 97
MATLAB® – Simulink model, 94
NP voltage ripple, 94–95
NTV strategy, 95, 96, 98
operating region, 96
switching-frequency, 99
switching sequences, 90
uncontrollable intervals, 84
waveforms, 84, 85
Battery charging mode, 3
Bidirectional DC/AC converter, 189–191
Bidirectional DC/DC converter, 190, 191
Bilinear Tustin transformation, 121, 156
Bode diagrams
closed loop, 158, 159
$I_L/V_u$, 158
$K(z)G(z)$
computation time delay, 153, 154
controller design, 155–157
output impedance, 194
RC control, 177, 178

© 2014 John Wiley & Sons, Ltd. Published 2014 by John Wiley & Sons, Ltd.
Companion Website: www.wiley.com/go/sharkh
Cascaded H-bridge (CHB) inverters, 264–267

Computational time delay
- $K(z)G(z)$ bode diagram, 153, 154
- $K(z)G(z)$ root locus, 153, 154
- PWM carrier, 151
- sampling strategy, 151, 152

Conduction losses, 54
- CHB inverter, 63–64
- high switching frequency, 58–59
- IGBT and diode, 59, 60
- inverter semiconductor, 59
- NPC 3L inverter
  - duty cycles, 61, 62
  - intervals, 61, 62
  - inverter diodes, 62–63
  - inverter IGBTs, 61
  - three-phase NPC, 63
  - pulse-by-pulse analysis, 59
  - two-level inverter, 60–61

Connection mode, 2–3

Controllable intervals (CIs), 82, 84

Controller area network (CAN), 162, 209

Converter topologies
- CHB converter
  - DC-link voltage, 15, 17
  - Simulink model, 27
  - switching states and conduction paths, 15–16, 18
- MATLAB® functions, 27
- NPC converter
  - phase voltage, 15
  - Simulink model, 26
  - switching modules, 14–15
  - switching states and conduction paths, 15, 16
- PWM (see Pulse width modulation (PWM))
  - two-level (2L) converter
    - Simulink model, 25

switching states and conduction paths, 13–14
- three-phase 2L converter, 13, 14

Coordination time interval (CTI), 246, 249

Current-controlled mode, 186

DC-link capacitors
- band-NV strategy, 83
- current harmonics, 47
  - CHB inverter, 39–41
  - Fourier analysis, 37–38
  - geometric wall model, 37, 38
  - NPC inverter, 38–39
  - current RMS expression
    - average and rms values, 32
    - CHB inverter, 39–41
    - IGBT-diode module, 32
    - inverter IGBT-diode module, 32
    - NPC inverter (see Three-level neutral-point-clamped (3L NPC) inverter)

- ESR, 29, 46–47
- higher-level inverters, 48
- ML inverter design, 29

numerical derivation
- current rms value, 41, 42
- MATLAB code, 281–284
- voltage ripple amplitude, 42, 43

- NV strategy, 82
- simulation results
  - MATLAB®–Simulink, 42, 68, 264–267
  - NPC and CHB inverter, 42–43, 45–46
  - operating parameters, 43, 44
  - spectrum, 44, 45

- sizing, 30–32
  - two- and three-level inverter topologies
    - average and rms values, 65
Index

CHB inverter, 68
  current rms expression, 67
derivation, 65–66
IGBT-diode module, 65
lower capacitor, 68
MATLAB®–Simulink, 68
NPC inverter, 67, 68
  switching intervals, 66
symmetrical sectors, 68
DC-link voltage controller, 190, 192
  block diagram, 206, 207
closed loop poles, 207, 208
DC/DC converter power, 206–207
open loop transfer function, 207
steady-state error, 209
step response, 207, 208
transient response, 213, 215
Digital sampling strategy, 113–115
Distributed generator (DG) systems, 185
  control and system issues
    capacitors, 8
computational time delay, 9
digital controller, 9
feedback loop structure, 7–8
filter resonance, 8
microprocessor-based controller, 7
power angle control, 7
converter topologies
  current source converter, 6
interleaving, 5–6
LCL filter, 4
matrix converter, 6
NPC inverter, 4–5
  switching frequency, 4
hysteresis modulation, 6–7
microgrid converters, 2–3
PDM, 7
PWM, 7
Energy storage
  grid-connected mode, 185
  line interactive UPS (see Line interactive UPS)
stand-alone mode, 185
Equivalent series resistance (ESR), 29, 46–47
Feedback loop structure, 7–8
Fuse saving strategy, 239
  adaptive algorithm
    communication link, 251
    fault currents, 251–252
    flow chart, 251, 253
    recloser operating time, 252, 255, 256
    TCC, 252, 254
CTI, 249
fault currents, 247
  \( I_{\text{pickup}} \) selection, 249–251
operating time, 248, 249
recloser fast curve modification, 248
recloser TCC modifications, 247–248
Geometric wall model, 37, 38
Grid-connected interleaved inverter
  advantages, 132
controller design
    bilinear Tustin transformation, 156
    closed loop Bode diagram, 158, 159
    grid disturbance rejection, 156
    grid harmonics rejection, 154–156
    grid impedance variation, 154, 156
    \( I_L/V_u \) Bode diagram, 158
    \( K(z)G(z) \) Bode diagram, 155–157
    phase lag compensator, 155, 156, 158

287
Grid-connected interleaved inverter (continued)
reference signal tracking, 154–156
root locus, 156, 157
controller structure
Hall-effect sensor, 147
natural damped frequency, 149
PWM inverter, 146, 148
time delay, 149
total inductor current, 149
filter capacitors, 134
filter resonance frequency, 134
hardware design
attenuation ratio, 144, 146
channel inductance, 137
copper losses, 144
core losses, 144
core size factor, 145
epcos cores data, 145
equivalent circuit diagram, 140, 142
filter capacitance, 137, 144
flowchart, 138, 139
IGBT/diode modules, 143–144
inductance, 138
inductor core and coil, 137
inductor current simulation, 140, 143
inductor number of turns, 144
inductor power losses, 146, 148
inductor size, 137–138
inductor stored energy, 145
interleaved channels, 137
inverter switching states, 140, 142
minimum inductor volume, 146, 147
peak-to-peak current, 140–141
switching frequency, 137
switching signals, 138, 141
switching states, 140, 142
total inductor rms current, 142
total inductor volume vs.
switching frequency, 145, 147
two-channel interleaved inverter, 138, 140
high power inverter disadvantages, 131
interleaving, 132
parallel multi-active power filters, 133
RC control (see Repetitive current (RC) control)
ripple cancellation
inductor ripple currents, 135
PCC, 135
peak-to-peak ripple current, 135–137
simulated capacitor current, 136–137
switching signals, 135
simulation and practical results
channel inductor current, 161
filter capacitor current, 159, 160
grid voltage and spectrum, 162, 165
grid voltage swell response, 161–162
grid voltage THD, 166–167
inductor interleaved currents, 162, 164
MATLAB®/Simulink model, 158
output current and spectrum, 162, 165
output current step response, 166–167
output current THD, 166–167
phases and inductor size, 161, 163
PWM outputs, 161–162
system parameters, 158, 159
three-phase output currents, 159–160, 162–163
TMS320F 2808 32-bit DSP, 161
total inductor current, 161
system analysis
  computational time delay, 151–154
  grid disturbance rejection, 154
  inductor current, 150
  passive damping and grid impedance, 151–152
  single channel equivalent block diagram, 150
  transfer function, 150
  zero order hold effect, 150
three-level inverter topology, 131–132
three-phase inverter diagram, 132, 133

Harmonic analysis, 38, 47
Hybrid modulation strategy
  CIs and UIs, 101
  flowchart, 101
  NPC converter, 100–101
  NP voltage, 100
Simulation results
  \( H_{\text{Sym-S3V}} \), 104
  NPC inverter, 102
  NTV strategy, 103
  NV and non-NV strategy, 105–106
  percentage duration, 104–105
  S3V strategy, 103
  waveforms, 102
  SPWM strategy, 100
  S3V, 100
Hysteresis modulation, 6–7
IGBT-diode modules, 53–54
Inner voltage feedback loop, 187

Line interactive UPS system, 209
  balanced and unbalanced three-phase system, 188
  battery charging to discharging mode transition, 213, 215
  bidirectional DC/AC converter, 189–191
  bidirectional DC/DC converter, 190, 191
circuit diagram, 189
classical topology, 185
control algorithm, 186–187
core controller
  block diagram, 191, 192
  closed loop transfer function, 192
  output voltage, 192
  system output impedance, 192
  virtual impedance and grid harmonics rejection, 193–194
DC-link voltage controller, 190, 192
  block diagram, 206, 207
  closed loop poles, 207, 208
  DC/DC converter power, 206–207
  open loop transfer function, 207
  steady-state error, 209
  step response, 207, 208
  transient response, 213, 215
feedback and feedforward loops, 192
frequency and voltage drooping methods, 187
grid-connected to stand-alone mode transition, 210–214
grid voltage, 216–217
low pass filter, 187–188
output current and bus voltage, 216–217
with virtual impedance, 216–217
power flow controller (see Power flow controller)
series-parallel topology, 185–186
stand-alone to grid-connected transition, 213, 214

MATLAB® functions, 27
MATLAB® SimPowerSystems, 178
MATLAB®/Simulink models
  band-NV strategy, 94
  grid-connected interleaved inverter, 158
NPC converter
  band-NTV strategy, 267, 270
  band-NV PWM generator block code, 267, 271–279
  DC-link capacitor rms current, 42, 68, 264–267
  NPS circuit, 267, 269
  peak–peak voltage ripple, 264–267
  vector selection block, 267, 268
three-phase two-level grid-connected inverter, 121
Microgrid converters
  battery charging mode, 3
  connection mode, 2–3
  stand-alone mode, 3
Microgrid system
  experimental results
    CAN protocol, 209
    controller parameter values, 209, 211
    experimental set-up, 209, 210
  structure, 187, 188
  anti-islanding controller, 189
  DG units, 188–189
  line interactive UPS (see Line interactive UPS system)
    STS, 188–189
    supervisory controller, 188
Nearest vectors (NV) strategy
  band-NV strategy (see Band-NV strategy)
  locally averaged NP current, 78–79
  lower boundary
    controllable intervals, 82
    DC-link capacitors, 82
    fundamental cycle, 81, 82
  uncontrollable intervals, 82
  waveforms, 81, 83
  operation, 77–78
  switching constraints, 79–81
  zero-ripple region, 81
Neutral point clamped (NPC) converter,
  see also Three-level neutral-point-clamped (3L NPC) converter
  duty cycles calculation, nearest space vectors, 261–262
MATLAB®–Simulink models
  band-NTV strategy, 267, 270
  band-NV PWM generator block code, 267, 271–279
  DC-link capacitor rms current, 264–267
  NPS circuit, 267, 269
  peak–peak voltage ripple, 264–267
  vector selection block, 267, 268
symmetric modulation strategy, 262–263
Neutral point clamped (NPC) inverter, 4–5
Open loop transfer function, 115
Outer active and reactive power sharing loop, 187
Padé approximation, 199
Phase-disposition pulse width modulation (PD PWM), 38, 39
Point of common coupling (PCC), 135, 186
Power flow controller
  drooping coefficient selection
    energy transient response, 201–203, 205–206
    frequency drooping coefficient, 201–202
    integral coefficient, 200, 202, 204
    maximum transient energy, 204
steady-state error, 205
trip limit, 202
voltage amplitude drooping coefficients, 204
drooping control equations, 195–196
root locus diagram
active power model, 200
reactive power model, 200, 201
small signal analysis
active and reactive power, 196–198
grid frequency and voltage reference, 197
grid impedance, 196
Padé approximation, 199
power measurement filters response, 199
time delay, 199
transfer function, 197–198
voltage reference, 195
Protection coordination
distribution network with distributed generation, 242, 243
fuse saving strategy (see Fuse saving strategy)
grid network upstream, 244
IEEE/ANSI designated protective device numbers, 244–245
impedance values, 245
interrupting device, 239
objective, 239
observations, 255–257
preventive solutions, 240–241
recloser and fuse coordination, 240
recloser application, 252, 254–255
recloser–fuse miscoordination, 240
remedial solutions, 241–242
selectivity, 239
simulation results
CTI, 246
fault current magnitudes, 245, 247
feeder LF1–1 length, 247
operating times, 246, 248, 249
recloser and fuse time coordination, 245, 246
reference point (RP), 246
TCC curve, 239–240
Thevenin equivalent circuit, 244
wind turbines, 244
Pulse density modulation (PDM), 7
Pulse width modulation (PWM)
carrier-based strategy
carrier waveform, 18, 19
CHB converter, 20
common-mode component, 21
line voltages, 21
phase disposition, 19, 20
pulsed phase voltages, 20
reference waveform, 17, 19
SPWM and unity modulation index, 17–18
third harmonic injection, 21, 22
SVM strategy
carrier-based implementations, 22
3L NPC converter, 24, 26
SV diagrams, 24, 26
transformation, 22
two-level converter, 22–24
voltage reference vector, 24, 25
$P–\omega$ and $Q–V$ droop control, 186–187
RC control, see Repetitive current (RC) control
Recloser and fuse coordination (RFC), 240–241
Recloser–fuse miscoordination, 240–241
Repetitive current (RC) control
experimental results
current THD, 181–182
output current, 181
proposed controller, 179
PWM counter, 179–180
RC implementation, 180–181
synchronization, 180
high bandwidth requirement, 172
Repetitive current (RC) control
(continued)
LCL output filter, 172
proportional-resonant controllers, 171
proposed controller and system
modeling
block diagram, 172, 173
inductor current, 173
natural resonance frequency, 174
simplified block diagram, 175
single channel equivalent, 175
system parameter, 174
repetitive feedback control, 171
simulation results, 178–180
system analysis and controller design
Bode diagram, 177, 178
disturbance transfer function, 178, 179
harmonics rejection, 175–176
normalized frequency response,
176–177
open loop transfer function, 176
Thevenin equivalent circuit, 244
Three-level cascaded H-bridge (3L
CHB) inverters
current harmonics, 39–41
current RMS expressions, 36–37
vs. NPC inverters, 45–46
simulation results, 42–43
Three-level neutral-point-clamped (3L
NPC) converter
advantage and disadvantage, 73
capacitor balancing, 73
modulation strategy
effective switching frequency, 76
hybrid strategy (see Hybrid
modulation strategy)
NV and non-NV strategy, 75–77
NV strategy (see Nearest vectors
(NV) strategy)
space vector diagram, 74–75
triplets, 75
NP voltage, 73/vue imbalance, 74
Three-level neutral-point-clamped (3L
NPC) inverter
vs. CHB inverters, 45–46
conduction losses
duty cycles, 61, 62
intervals, 61, 62
inverter diodes, 62–63
inverter IGBTs, 61
three-phase NPC, 63
current RMS expression
AC component, 33
duty cycle, 34
inverter modulation index, 33
switching intervals, 35
symmetry, 36
upper modules, 34
harmonic analysis, 38–39
simulation results, 42–43
SVM strategy, 24, 26
switching losses, 57

Sinusoidal pulse width modulation
(SPWM), 17–18
Space vector modulation (SVM), 7
Stand-alone mode, 3, 185
Static transfer switch (STS), 188–189
Steinmetz equation, 144
Switching losses
CHB 3L inverter, 57
frequency, 54
NPC 3L inverter, 57
two-level inverters
fundamental period, 55–56
IGBTs and diodes, 54–56
interleaved inverter losses, 56
inverter semiconductor, 55
power loss expression, 56
power semiconductors, 56
turn-on and turn-off energy loss,
54, 55

Three-level cascaded H-bridge (3L
CHB) inverters
current harmonics, 39–41
current RMS expressions, 36–37
vs. NPC inverters, 45–46
simulation results, 42–43
Three-level neutral-point-clamped (3L
NPC) converter
advantage and disadvantage, 73
capacitor balancing, 73
modulation strategy
effective switching frequency, 76
hybrid strategy (see Hybrid
modulation strategy)
NV and non-NV strategy, 75–77
NV strategy (see Nearest vectors
(NV) strategy)
space vector diagram, 74–75
triplets, 75
NP voltage, 73/vue imbalance, 74
Three-level neutral-point-clamped (3L
NPC) inverter
vs. CHB inverters, 45–46
conduction losses
duty cycles, 61, 62
intervals, 61, 62
inverter diodes, 62–63
inverter IGBTs, 61
three-phase NPC, 63
current RMS expression
AC component, 33
duty cycle, 34
inverter modulation index, 33
switching intervals, 35
symmetry, 36
upper modules, 34
harmonic analysis, 38–39
simulation results, 42–43
SVM strategy, 24, 26
switching losses, 57

Sinusoidal pulse width modulation
(SPWM), 17–18
Space vector modulation (SVM), 7
Stand-alone mode, 3, 185
Static transfer switch (STS), 188–189
Steinmetz equation, 144
Switching losses
CHB 3L inverter, 57
frequency, 54
NPC 3L inverter, 57
two-level inverters
fundamental period, 55–56
IGBTs and diodes, 54–56
interleaved inverter losses, 56
inverter semiconductor, 55
power loss expression, 56
power semiconductors, 56
turn-on and turn-off energy loss,
Three-phase two-level grid-connected inverter

capacitor current observer
characteristic equation, 118
observer pole, 118
simulation, 119
state space model, 117–118
transfer function, 116
z-domain, 116, 117
z-transform, 117
circuit diagram, 110
control strategy, 112–113
digital sampling strategy, 113–115
experimental results
capacitor current, 124, 126
grid voltage, 123–125
output current, 124, 127
feedback controllers
frequency plot, 119, 120
inner and outer loop controller,
119, 120
phase lag compensator, 121, 122
Tustin bilinear transformation, 121
LCL filter topology, 109, 110
microprocessors/DSPs, 109
natural damped frequency, 111
PWM, 111
simulation results
capacitor and output current, 121, 123, 124
MATLAB®–Simulink model, 121
THD, 122, 125
time delay observer, 121, 122
utility voltage harmonics, 123
system parameter and component values, 110, 111
time delay effect, 115–116
undamped natural frequency, 111
Time–current coordination (TCC) curve, 239–240
Total harmonic distortion (THD), 131
Two- and three-level inverter topologies
circuit diagrams, 51, 52
conduction losses (see Conduction losses)
DC-link capacitor
average and rms values, 65
CHB inverter, 68
current rms expression, 67
derivation, 65–66
lower capacitor, 68
MATLAB®–Simulink, 68
NPC inverter, 67, 68
switching intervals, 66
symmetrical sectors, 68
ESR, 69, 70
IGBT-diode modules, 53–54, 65
low-frequency harmonics, 70
semiconductor losses vs. inverter modulation index, 69
switching losses (see Switching losses)

Uncontrollable intervals (UIs), 82, 84
Uninterruptible power supply (UPS) systems, see Line interactive UPS system

Voltage-controlled mode, 186

Zero-ripple region, 81