## Contents

**About the Author**  
xiii  
**Preface**  
xv  

1  **SiP Design and Simulation Platform**  
1.1 From Package to SiP  
1.2 The Development of Mentor SiP Design Technology  
1.3 The Mentor SiP Design and Simulation Platform  
1.3.1 SiP Platform Introduction  
1.3.2 Schematic Input  
1.3.3 Concurrent System Design  
1.3.4 SiP Board Design  
1.3.5 Signal Integrity and Power Integrity Simulation  
1.3.6 Thermal Analysis  
1.3.7 The Advantages of the Mentor SiP Design and Simulation Platform  
1.3.7.1 Characteristics of Mentor SiP Design and Simulation Platform  
1.3.7.2 Design Areas of Mentor SiP Design and Simulation Platform  
1.4 The Introduction of the Finished Project  

2  **Introduction to Package**  
2.1 Definition and Function of Package  
2.2 Development of Packaging Technology  
2.3 SiP and Related Technologies  
2.3.1 The Appearance of SiP Technology  
2.3.2 SoC and SiP  
2.3.3 SiP-Related Technologies  
2.4 The Development of the Package Market  
2.5 Package Manufacturers  
2.5.1 Traditional Package Manufacturers  
2.5.2 New SiP Manufacturers in Different Areas  
2.6 Bare Chip Suppliers  

3  **The SiP Production Process**  
3.1 BGA: The Mainstream SiP Package Form  
3.2 The SiP Package Production Process  
3.3 Three Key Elements of SiP
4 New Package Technologies 45
4.1 TSV (Through Silicon Via) Technology 45
4.1.1 TSV Introduction 45
4.1.2 TSV Technical Characteristics 46
4.1.3 TSV Application and Prospects 48
4.2 Integrated Passive Device (IPD) Technology 49
4.2.1 IPD Introduction 49
4.2.2 The Advantages of IPD 50
4.3 Package on Package (PoP) Technology 51
4.3.1 The Limitations of 3D SiP 51
4.3.2 The Application of PoP 52
4.3.3 The Emphasis in PoP Design 54
4.4 Apple A8 processor – an Example of a PoP Product 55

5 SiP Design and Simulation Flow 59
5.1 SiP Design and Simulation Flow 59
5.2 Design and Simulation Process in Mentor EE Flow 61
5.2.1 Library Creation 61
5.2.2 Schematic Design 62
5.2.3 Layout Design 63
5.2.4 Design Simulation 66

6 Central Library 67
6.1 The Structure of the Central Library 67
6.2 Introduction to the Dashboard 68
6.3 Schematic Symbol Creation 70
6.4 Bare Chip Cell Creation 76
6.4.1 Create Bare Chip Padstack 76
6.4.2 Create Bare Chip Cell 78
6.5 BGA Cell Creation 82
6.5.1 Create BGA Padstack 82
6.5.2 Create BGA Cell Manually 84
6.5.2.1 Tips for Renaming the Pin Numbers 87
6.5.2.2 View Layers Defined in Padstacks 87
6.5.3 Create BGA Cell with Die Wizard 88
6.5.4 LP Wizard Professional Library Tool 89
6.6 Part Creation 90
6.7 Create Cell Via Part 92

7 Schematic Input 97
7.1 Netlist Input 97
7.2 Basic Schematic Input 99
7.2.1 Start DxDesigner 99
7.2.1.1 General Toolbar 100
7.2.1.2 Digital/analog Simulation Toolbar 105
7.2.1.3 RF Circuit Design Toolbar 105
## Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.2.2</td>
<td>Create New Project 105</td>
</tr>
<tr>
<td>7.2.2.1</td>
<td>How to Create a New Project 105</td>
</tr>
<tr>
<td>7.2.2.2</td>
<td>Net Connection and Draw Toolbar 108</td>
</tr>
<tr>
<td>7.2.3</td>
<td>Schematic Design Check 110</td>
</tr>
<tr>
<td>7.2.4</td>
<td>Design Rules Setup 110</td>
</tr>
<tr>
<td>7.2.5</td>
<td>Package Design 112</td>
</tr>
<tr>
<td>7.2.5.1</td>
<td>Packaging Options 113</td>
</tr>
<tr>
<td>7.2.5.2</td>
<td>PDB Extraction Options 114</td>
</tr>
<tr>
<td>7.2.6</td>
<td>Partlist Output 115</td>
</tr>
<tr>
<td>7.2.7</td>
<td>Chinese Input in Schematic 117</td>
</tr>
<tr>
<td>7.2.8</td>
<td>Enter Layout Environment 118</td>
</tr>
<tr>
<td>7.3</td>
<td>Schematic Input Based on DxDataBook 120</td>
</tr>
<tr>
<td>7.3.1</td>
<td>DxDataBook Introduction 120</td>
</tr>
<tr>
<td>7.3.2</td>
<td>DxDataBook Usage 121</td>
</tr>
<tr>
<td>7.3.3</td>
<td>Check and Update Component Properties 123</td>
</tr>
<tr>
<td>8</td>
<td>Multi-board Project Management and Concurrent Schematic Design 127</td>
</tr>
<tr>
<td>8.1</td>
<td>Multi-Board Project Management 127</td>
</tr>
<tr>
<td>8.1.1</td>
<td>SiP and PCB Collaborative Design 127</td>
</tr>
<tr>
<td>8.1.2</td>
<td>Multi-Board Project Design Flow 128</td>
</tr>
<tr>
<td>8.2</td>
<td>Concurrent Schematic Design 130</td>
</tr>
<tr>
<td>8.2.1</td>
<td>Concurrent Design Thinking 130</td>
</tr>
<tr>
<td>8.2.2</td>
<td>Operating Method for Concurrent Schematic Design 131</td>
</tr>
<tr>
<td>9</td>
<td>Layout Creation and Setting 137</td>
</tr>
<tr>
<td>9.1</td>
<td>Create Layout Template 137</td>
</tr>
<tr>
<td>9.1.1</td>
<td>Layout Template Definition 137</td>
</tr>
<tr>
<td>9.1.2</td>
<td>Create SiP Layout Template 137</td>
</tr>
<tr>
<td>9.2</td>
<td>Create Layout Project 146</td>
</tr>
<tr>
<td>9.2.1</td>
<td>Create New SiP Project 146</td>
</tr>
<tr>
<td>9.2.2</td>
<td>Enter Layout Design Environment 148</td>
</tr>
<tr>
<td>9.3</td>
<td>Layout-Related Setup and Operation 149</td>
</tr>
<tr>
<td>9.3.1</td>
<td>Introduction to Layout License Control 149</td>
</tr>
<tr>
<td>9.3.2</td>
<td>Mouse Handling 152</td>
</tr>
<tr>
<td>9.3.3</td>
<td>Three Kinds of Commonly used Operating Modes 153</td>
</tr>
<tr>
<td>9.3.3.1</td>
<td>Select Parts 156</td>
</tr>
<tr>
<td>9.3.3.2</td>
<td>Select Nets 157</td>
</tr>
<tr>
<td>9.3.3.3</td>
<td>Select Draw Objects 158</td>
</tr>
<tr>
<td>9.3.4</td>
<td>Display Control 160</td>
</tr>
<tr>
<td>9.3.4.1</td>
<td>Layer Tab, General Tab, Part Tab 161</td>
</tr>
<tr>
<td>9.3.4.2</td>
<td>Net Tab, Hazard Tab, Groups Tab 165</td>
</tr>
<tr>
<td>9.3.5</td>
<td>Editor Control 166</td>
</tr>
<tr>
<td>9.3.5.1</td>
<td>Common Settings 166</td>
</tr>
<tr>
<td>9.3.5.2</td>
<td>Place Tab 169</td>
</tr>
<tr>
<td>9.3.5.3</td>
<td>Route Tab 169</td>
</tr>
<tr>
<td>9.3.5.4</td>
<td>Grids Tab 173</td>
</tr>
<tr>
<td>9.3.6</td>
<td>Setup Parameters 174</td>
</tr>
<tr>
<td>9.4</td>
<td>Substrate Layout 174</td>
</tr>
</tbody>
</table>
9.4.1 Component Placement 174
9.4.2 Automatic Optimization of Net Connections 176
9.5 eDxD View 177
9.6 Input Chinese Characters in Layout 178
9.6.1 Manually Input Chinese Characters 178
9.6.2 Import Chinese Words from DXF File 179

10 Constraint Rules Management 183
10.1 CES – Constraint Editor System 183
10.2 Scheme 185
10.2.1 Create Scheme 185
10.2.2 Use Scheme in Layout 186
10.3 Define Layer Stackup and Parameters 187
10.4 Net Class 188
10.4.1 Create Net Class and Assign Nets to Net Class 188
10.4.2 Define Net Class Rules 188
10.5 Clearance Rules 190
10.5.1 Clearance Rule Creation and Setup 190
10.5.2 General Clearance Rules 192
10.5.3 Net Class to Net Class Clearance Rules 193
10.6 Constraint Class 194
10.6.1 Create Constraint Class and Assign Net to Constraint Class 194
10.6.2 Constraint Classes Classification 194
10.6.3 Edit Constraint Groups 198
10.7 Update CES Data with Layout 200

11 Wire Bond Design 201
11.1 Wire Bond Overview 201
11.2 Bond Wire Model 203
11.2.1 Bond Wire Model Creation 203
11.2.2 Bond Wire Properties 207
11.3 Wire Bond Toolbar 209
11.3.1 Add Bond Wire Manually 209
11.3.2 Move and Rotate Bond Pad 210
11.3.3 Wire Bond and Power Ring Generator 211
11.3.4 Wire Bond Rule Setting 213
11.3.4.1 Settings for Part 213
11.3.4.2 Settings for Die Pin 217
11.3.4.3 Add Multiple Bond Wires between Die Pin and Bond Pad 219
11.3.4.4 Fan Out to Multiple Bond Pads from Single Die Pin 220
11.3.4.5 Bond Multiple Die Pins to One Bond Pad 220
11.3.4.6 Die-to-Die Bonding 221
11.3.5 Wire Model Editor 222

12 Cavity and Chip Stack Design 229
12.1 Cavity 229
12.1.1 Cavity Definition 229
12.1.2 Cavity Creation 230
12.1.3 Place Component into Cavity 231
12.1.4 Bonding in Cavity 234
12.1.5 Embedded Cavity Design and Embedding Chip into Substrate 236
12.2 Chip Stack 239
12.2.1 The Concept of Chip Stack 239
12.2.2 Chip Stack Creation 241
12.2.3 Stack Chips Side by Side 243
12.2.4 Adjust Relative Position of Chips in Stack 244
12.2.5 Chip Stack Bonding 244

13 Flip Chip and RDL Design 249
13.1 The Concept and Characteristics of Flip Chip 249
13.2 The RDL Concept 250
13.3 RDL Design 250
13.3.1 Create Bare Die and RDL Library 251
13.3.2 RDL Schematic Design 254
13.3.3 RDL Layout Design 254
13.4 Flip Chip Design 260
13.4.1 Flip Chip Schematic Design 261
13.4.2 Flip Chip Layout Design 262

14 Route and Plane 269
14.1 Routing 269
14.1.1 Introduction to Routing 269
14.1.2 Manual Route 269
14.1.3 Plow Modes 270
14.1.4 Gloss Modes 272
14.1.5 Fix and Lock 273
14.1.6 Layer Switching 273
14.1.7 Move Trace and Via 275
14.1.8 Circuit Copy 276
14.1.9 Semi-Automatic Route 278
14.1.10 Auto Route 279
14.1.11 Route Differential Pairs 281
14.1.12 Length Control in Routing 284
14.2 Plane 291
14.2.1 Plane Definition 291
14.2.2 Plane Setting 291
14.2.2.1 Plane Classes Parameters 291
14.2.2.2 Plane Assignments 294
14.2.3 Draw Plane Shape 296
14.2.4 Modify Plane Shape 298
14.2.5 Generate Negative Plane Data 300
14.2.6 Delete Plane Data 300
14.2.7 Verify Plane Data 301
15 Embedded Passives Design 303
15.1 The Development of Embedded Technology 303
15.1.1 Discrete Embedded Technology 303
15.1.2 Planar Embedded Technology 303
15.2 Process and Material for Embedded Passives 305
15.2.1 Embedding Processes 306
15.2.1.1 Additive Resistors 307
15.2.1.2 Subtractive Resistors 309
15.2.1.3 Capacitors 310
15.2.2 Embedding Materials 314
15.2.2.1 Capacitor Materials 314
15.2.2.2 Conductor Materials 314
15.2.2.3 Insulator Materials 316
15.2.2.4 Resistor Materials 316
15.2.3 The Nonlinear Characteristics of Resistance Materials 318
15.3 Resistor and Capacitor Automatic Synthesis 319
15.3.1 Preparation for Automatic Synthesis 319
15.3.2 Resistor Automatic Synthesis 322
15.3.3 Capacitor Automatic Synthesis 325

16 RF Circuit Design 331
16.1 RF SiP Technology 331
16.2 Mentor RF Design Flow 332
16.3 RF Schematic Design 333
16.3.1 RF Shapes Library Configuration 333
16.3.2 RF Schematic Toolbar 334
16.3.3 RF Schematic Design 340
16.4 RF Parameter Transfer Between Schematic and Layout 342
16.5 RF Layout Design 344
16.5.1 RF Toolkit in Layout 345
16.5.2 Three Kinds of RF Unit 349
16.5.3 Add and Edit Meander 350
16.5.4 RF Control Window 353
16.5.5 Create Custom RF Shape 355
16.5.6 RF Via 355
16.5.7 RF Group 357
16.5.8 Other RF Edit Functions 359
16.6 Connect RF Simulation Tools and Transfer Data 363
16.6.1 Connect RF Simulation Tools 363
16.6.2 Layout RF Data Transmission 364
16.6.3 Schematic RF Data Transmission 365

17 Concurrent Layout Design 367
17.1 Concurrent Layout Design Technology – Xtreme 367
17.2 Xtreme Configuration 369
17.3 Start Xtreme Concurrent Design 371
17.4 Matters to Note in Xtreme 375

18 3D Real-time DRC 377
18.1 Wire Model Editor 3D Display and DRC 377
18.1.1 Wire Model Editor 3D display 377
18.1.2 Wire Model Editor 3D DRC 378
18.2 3D Viewer Display and DRC 380
18.2.1 3D Viewer Introduction 380
18.2.2 Real-Time Check in 3D Viewer 383
18.2.3 3D Simulation of SiP Production Processing 384
18.2.4 Import 3D Mechanical Data 387
18.2.5 Real-time DRC in 3D Viewer 390

19 Design Review 395
19.1 Online DRC 395
19.2 Batch DRC 395
19.2.1 DRC Settings 396
19.2.2 Connectivity and Special Rules 399
19.2.3 Batch DRC Scheme 401
19.3 Review Hazards 401
19.4 Verify Design Library 403

20 Manufacturing Data Output 407
20.1 Drill and Gerber Data Output 407
20.1.1 Drill Data Output 407
20.1.2 Gerber Machine Format 411
20.1.3 Gerber Data Output 411
20.1.4 Import and Check Gerber Data 416
20.2 Other Manufacturing Data Output 416
20.2.1 Component and Bond Wire Coordinate File Output 416
20.2.2 DXF File Export 420
20.2.3 Layout Design Status Output 420
20.2.4 BOM Output 421

21 SiP Simulation Technology 425
21.1 SiP Simulation Technology Overview 425
21.2 Signal Integrity Simulation 426
21.2.1 HyperLynx SI Simulation Tool Introduction 427
21.2.2 HyperLynx SI Simulation Example 430
21.3 Power Integrity Simulation 436
21.3.1 HyperLynx PI Simulation Tool Introduction 439
21.3.2 HyperLynx PI Simulation Example 441
21.4 Thermal Analysis 443
21.4.1 HyperLynx Thermal Introduction 447
21.4.2 HyperLynx Thermal Simulation Example 448
21.5 EMI/EMC Analysis 457
  21.5.1 HyperLynx DRC Introduction 457
  21.5.2 HyperLynx DRC Example 459
21.6 Mixed-Signal Simulation Introduction 462

Reference Materials 467

Postscript and Thanks 469

Index 471