Index

A
adaptive block redundancy, 63. see also single crystal silicon stacked
ALD - atomic layer deposition, 78
array efficiency, 202, 220, 221
Arrhenius Curve, 114
a-Si (amorphous silicon), 47, 60, 82, 83, 112
asperities (silicon protrusions). see flash memory
AXI (advanced extensible interface), 286

B
backtunneling, 72, 73, 77
band diagram (diagram plotting electron energy levels vs. a spatial dimension), 31
bandgap engineer (BE), 49, 51–52, 53, 54, 136, 165
BE. see bandgap engineer
BEOL (back end of the line), 299, 301
BE-SONOS NAND, 165, 167–169
BiCS (bit cost scalable). see vertical channel NAND
bipolar switching, 20, 199. see also ReRAM with selector, 246–256
selectorless, 208–216
BISR (built in self repair), 316–318
BIST (built in self test), 64, 316, 318
bit-line decode, 99. see also SSL decode
blocking layer, 15, 72, 73, 77
butterfly curves, 59. see also SNM

C
CAD (computer automated design), 275
carbon nanotube (CNT), 203, 206, 207, 240–241, 257
chalcogenide, 238. see also Phase Change Memory (PCM)
Charge trapping (CT), 14, 72–115, 119–146. see also SONOS
charge spreading, 143, 146
EAROM (see MNOS)
MNOS, 14, 15
SONONS, 128
SONS, 107
CHEI (channel hot electron injection), 13, 14, 29, 30, 73
CMOS (Complementary Metal Oxide Silicon), 2, 129
CMP (chemical mechanical planarization), 28
CMS. see complementary resistive switching
CNT. see carbon nanotube
complementary resistive switching (CRS), 256–266
compliance current. see ReRAM
Conductive Bridge RAM (CB-RAM), 205, 225, 226, 259
conductive filament. see ReRAM
copper pumping, 299. see also TSV Proximity effects
coupling ratio, 28, 29
cross-bar array. see cross-point array

cross-point array, 20–21, 192–269

horizontal, 196

non-linear effect, 215–217, 218

parasitic conducting paths, 208

parasitic resistance, 201, 203, 212–215

passive, 208

selectorless, 208–227

self rectifying, 216

vertical, 196

crystal orientation, 27

CT. see charge trapping

D

Damascene process, 28, 62

data self-aligners, 320–321

DC-SF (dual control gate with surrounding floating gate). see Vertical Floating Gate NAND Flash

DDR (double data rate), 8, 277

declare. see SSL decode

depletion mode (transistor normally on), 14

DIBL (drain induced barrier lowering), 27, 84, 238. see also GAA

DIGBIL. see grain boundary effects

disturb

gate, 30

program, 22, 30, 31, 119

read, 30, 31

double data rate. see DDR

double gate, 37, 42–43 162, 163–189

drain induced barrier lowering (DIBL).

see DIBL

DRAM, 1, 5–11

cube (see memory cube)

embedded, 10–11

folded bank architecture, 308–310

operation, 6–11

stack capacitor, 6, 8, 9

trench capacitor, 6, 8–11

DSSB - (dopant segregated schottky barrier).

see flash memory

DUV (deep ultraviolet lithography), 39

dynamic RAM. see DRAM

E

EAROM (electrically alterable read only memory), 14. see also MNOS ROM

ECC (error correction code), 145, 282

EDA (electronic design automation), 285

EEPROM (electrically erasable programmable read only memory), 13, 15

two transistor (2T) pp. 13

EEPROM (electrically erasable read only memory), 15

effective cell size, 135

eFlash (embedded flash), 13, 14

electromechanical diode, 226–227

electromigration, 203, 206

electron back tunneling. (see flash memory)

embedded memory, 11–13

emerging memory, 22–23

EMI (electromagnetic interference), 12

energy efficiency (in TSV systems), 306–311

Engineered Tunneling Layer. see bandgap engineering

epitaxial diode, 228, 245

epitaxial layers. see single crystal silicon stacking

EPROM (erasable programmable read only memory), 13

eRAM (embedded RAM), 11–12

ESCG (extended sidewall control gate).

see Vertical Floating Gate NAND Flash

ESD (electro-static discharge), 12

etch profile / etch slope, 123, 163, 182–183

F

F^2 (feature size squared), 20

effective area, 123

FD-SOI (fully depleted - silicon on insulator), 26

FEOL (front end of the line), 301

ferroelectric RAM. see emerging memory

filamentary conduction, 195, 197.

see also metal-oxide ReRAM

FinFET, 1, 25

body tied flash, 28, 32

bulk silicon, 26, 28–34

crystal orientation, 27

double gate flash, 26

double gate vs. tri gate flash, 38, 39

Flash, 26–34, 37–39, 74

flash charge loss mechanisms, 31

independent double gate (IDG) flash, 42, 43

paired flash, 32–34, 43

SOI Silicon, 26–27

SRAM, 6

Transistor, 6, 25–26

Flash. see Flash Memory
Flash Memory, 13
asperities, 46
DSSB Flash, 39–42
electron back tunneling, 39
erase, 13
erase saturation, 39
floating gate, 119, 146–157
IDG TFT CT-, 43–45
TFT flash, 43–48
F minimum feature size, 227
FN Tunneling. see Fowler-Norheim tunneling
forming operation. see ReRAM
Fowler-Nordheim tunneling, 13, 81
poly-to-poly, 14
FPGA (field programmable gate array), 275, 333
Frenkel-Poole
current, 54
emission, 31
G
GAA (gate-all-around), 1, 16, 17, 72–116.
see also nanowire
DIBL, 84, 86
memory transients, 78–80
omega gate, 83
radial effects, 86, 129, 130, 136
side-gate, 84
subthreshold slope, 83
subthreshold swing, 86
gate-first, 130, 131
gate-last, 111
gate replacement process, 142
GIDL (gate induced drain leakage), 128
current, 133
erase, 142, 186
GIGBL. see grain boundary effects
global clock distribution, 282
grain boundary effects. see also vertical gate
NAND variability
DIGBL - drain induced grain barrier
lowering, 180–182
GIGBL - gate induced grain barrier
lowering, 180–182
traps, 157
graphene
NV memory channel, 48
wires, 206
ground bounce, 12
GSL (ground select line), 32
H
half-selected, 192, 193, 198
HHI (hot hole injection), 29, 73
HMC (hybrid memory cube). see memory cube
horizontal channel. see vertical gate
I
IDG (independent double gate). see FinFET IDG
flash; SSL decode; TFT IDG flash
ILD (interlayer dielectric), 48, 61
inductive coupling stacks, 333–339
intelligent signal processor array (iSPA), 285–286
interposers passive, 276, 292
I/O - input/output, 64
IPD (inter-poly-dielectric), 29, see also ILD
J
JEDEC, 277, 293
junctionless channel, 54, 119. see also nanowire
junctionless NAND string. see also nanowire
endurance, 95
erase saturation, 92
K
k (number) 1000, 282
k-bits (1024 bits), 242
κ dielectric constant
high κ, 6, 8, 29, 32, 48, 51, 72, 77
low κ, 30
L
LEG (lateral epitaxial silicon), 60–63
LP-CVD (low pressure chemical vapor
deposition), 30, 52, 61, 81
LRS/HRS current ratio, 216. see also ON/OFF
current ratio
M
MANOS, 114
MCGL (metal control gate last process).
see Vertical Floating Gate NAND Flash
MCU (microcontroller), 17
description, 17
footprint, 17
memory cube
DRAM, 307
hybrid (HMC), 277, 280, 281–282
memory hierarchy, 278, 287–290
memory wall, 1, 7
memristor, 208, 256
metal gate, 73, 77
workfunction, 73
metal-oxide ReRAM, 20, 195, 219
transition metal oxide, 195
microcontroller. see MCU
MIEC (mixed ionic electronic conduction), 228, 241–243
MIM (metal-insulator-metal), 228, 234
MLC. see multilevel cell
MNOS ROM (metal-nitride-oxide-silicon), 14, 15
MONOS (metal-oxide-nitride-oxide-silicon), 15.
see also SONOS
Moore’s Law 2
MOSFET (metal oxide silicon field effect transistor), 2
MRAM. see STT-MTJ
multi-bit cell, 90
multi-level
cell (MLC), 64, 88, 115, 122, 133, 145, 146, 154
transfer characteristics, 30

N
NAND flash, 17–20, 64–69
Operation, 19
nanocrystals, 35, 72, 74, 85–86
nanowire, 72–115. see also GAA
cell (MLC), 64, 88, 115, 122, 133, 145, 146, 154
transfer characteristics, 30

Q
Qs (charge density), 92

R
random telegraph noise. see RTN
random trap fluctuation. see RTF
redox (reduction-oxidation). see ReRAM
reduction-oxidation
redundancy analysis, 316–318
repartitioning, 279, 283
ReRAM (resistance RAM), 20, 23, 194
bipolar switching, 20, 196, 198, 246–286
compliance current, 199, 229, 235
conductive filament, 199–200
filamentary, 20
forming operation (filament forming), 199, 222, 224, 229
oxygen vacancies, 217 223, 251
reduction-oxidation (redox), 228, 230, 236
RESET (OFF state), 199
SET (ON state), 199
threshold switching, 246–247
unipolar switching, 20, 196, 198, 227–245
resistance RAM. see ReRAM
R_{HRS}/R_{LRS}. see R_{OFF}/R_{ON}
RIE (reactive ion etch), 78, 81, 127
R_{OFF}/R_{ON} (ratio of OFF state resistance to ON state resistance), 209, 216
RTF (random trap fluctuation), 144–145
RTN (random telegraph noise), 144–145, 157, 184
S
S3. see single silicon stacked salicide (self aligned silicide), 133
SANOS, 74
SB-CAT (square wave-shaped bit-line cell array transistor). see vertical channel NAND SBT (source body tied), 65
Schottky barrier, 234–237
Schottky diode selector, 252–254
Schottky emission, 31
SCP (sidewall control pillar). see vertical floating gate NAND flash
SDRAM, 1, 8, 9
select device/selector (device that controls a memory element), 197
diode selector, 201
selective epitaxial growth (SEG), 61. see also LEG
self-rectifying, 234, 235, 254–255
set-reset instability, 232
short channel effects, 25, 26, 50, 74
sic single crystal silicon. see nanowire - single crystal silicon
single-crystal silicon stacked (S3), 16, 56–69
NAND Flash, 64–69
SRAM, 57–64
SiNW (silicon nanowire). see nanowire, single crystal silicon
stacked SiNW, 96
SIP (system in package), 277
sloped etch, 103
sneak leakage, 193–194, 200, 209–211, 261
SNM (static noise margin), 4, 59
SoC (system-on-chip), 2, 12
SOI (silicon on insulator), 1, 26, 78
SONONS (silicon-oxide-nitride-oxide-nitride-silicon), 109
SONOS (silicon-oxide-nitride-oxide-silicon), 29, 73, 74. see also charge trapping SONS (silicon-oxide-nitride-silicon), 109
spin-RAM. see STT-MTJ
SRAM, 1, 3–6, 57–64
bit-line, 4
bit-line\), 4
BL (see bit-line)
BL\ (see bit-line)\
SSCG (separated sidewall control gate).
see Vertical Floating Gate NAND Flash
SSD - solid state drive, 19
SSHEI (source-side hot electron injection), 15
SSL (string select line), 32, 164
SSL decode
IDG SSL decode, 171–173
island gate decode, 176–177
multiple island gate decode, 169–171
PN decode, 168, 169
stacked NAND flash, see also nanowire fabrication, 96–98
horizontal SiNW, 96–97
program/erase characteristics, 97
single crystal, 98–101
STAR (stacked array architecture), 98–101
static noise margin. see SNM
static RAM. see SRAM
STI (stacked trench isolation), 30
edge fringing field, 34
storage class memory, 278, 289
string conductance, 124
STT-MTJ (spin torque transfer - magnetoresistive tunnel junction), 21–23, 36, 269–271
operation, 21–22
thermal stability, 36, 37
STT-RAM. see STT-MTJ
subthreshold
slope 96, 142
swing, 27
synchronous, 8
synchronous DRAM. see SDRAM
system footprint, 12
system Form Factor, 12
| TAHOS (TaN/Al₂O₃/ HfO₂/SiO₂/Si), 77, 86–87 |
| TANOS (TaN-Al₂O₃-SiN-SiOₓ-Si), 34, 66, 78, 109–110 |
| TCAD - technology computer aided design, 120 |
| TCAT (terrabit cell array transistor). see vertical channel |
| TEOS (Tetraethyl orthosilicate), 30 |
| testing (3D stacks), 316–320 |
| TFT (thin film transistor), 4, 15–16, 25, 43–48, 57, 82 |
| flash polysilicon protrusions, 46 |
| GAA CT memory, 82 |
| IDG flash, 43–45, 165–189 |
| variability, 55 |
| thermal expansion mismatch. see TSV proximity effects |
| thermal management |
| 3D systems, 314–316 |
| hot spots, 314 |
| thermal stability. see STT-MTJ |
| thin film transistor. see TFT |
| Three dimension. see 3D |
| threshold switching, 243, 263 |
| threshold vacuum switch (TVS), 251–252 |
| Threshold Voltage (Vₖh), 73 |
| Threshold Voltage Shift (ΔVₖh), 73, 86–87 |
| Threshold Voltage Window (ΔVₖh), 74 |
| through silicon via. see TSV |
| trap layer engineering, 85–86 |
| trigate -. see FinFET |
| TSV (through silicon via), 2, 13, 275–334 |
| 2.5D, 13, 292–293, 295 |
| 3D, 13, 293–294, 295 |
| dummy, 283 |
| FinFET technology, 324–326 |
| network platform, 331–332 |
| reconfiguring for performance, 326–329 |
| TSV processes |
| via first, 301–302 |
| via last, 299–302 |
| via middle, 302–305 |
| TSV proximity effects, 300, 325 |
| thermal expansion, 299, 300, 324 |
| thermal mechanical stress, 324, 326 |
| tunneling. see also Fowler-Nordheim, CHEI, HHI |
| trap-to-band, 89 |
| tunnel oxide, 74 |

| U |
| unipolar switching. see ReRAM |

<p>| V |
| vacuum tunneling layer, 47, 48 |
| Vanadium oxide selector, 228, 246 |
| variation (in 3D stacks), 320–321 |
| varistor bidirectional switch, 250–251 |
| vertical channel NAND, 119, 120, 123, 124–146 |
| BiCS, 110, 120, 121, 124–129 |
| P-BiCS, 120, 129–137 |
| SB-CAT, 145–146 |
| TCAT, 111, 120, 121, 142–145 |
| V-NAND, 138 |
| VRAT, 120, 138–139 |
| VSAT, 120, 121 |
| Z-VRAT, 138–141 |
| vertical floating gate NAND flash, 146–159 |
| DC-SF, 152–155 |
| decode (see SSL decode) |
| ESCG, 146–149 |
| MCGL, 153–155 |
| SCP, 155–157 |
| S-SCG, 149–152 |
| vertical gate NAND, 119, 123, 159–189 |
| band-to-band program, 185 |
| BE-SONOS, 120–189 |
| bit-alterable, 187 |
| channel boosting, 186 |
| channel self boosting, 178 |
| decode, 159 (see also SSL decode) |
| double gate, 162–163 |
| horizontal channel, 124 |
| program disturb, 179 |
| read disturb, 178–179 |
| shift BL scramble, 176–177 |
| staircase contact, 176 |
| variability, 180–182 |
| z-disturb, 178–180, 184 |
| vertical pipe,. see vertical channel |
| vertical polysilicon NAND, 107–114 |
| cost analysis, 116 |
| gate replacement, 111–112 |
| vertical single silicon channel, 49 |
| vertical single silicon NAND string, 105–107 |
| virtual source/drain, 91. see also nanowire |
| junctionless |
| VNAND (vertical NAND), 111. see also TCAT |</p>
<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>V-NAND (vertical NAND)</td>
<td>see vertical channel NAND</td>
</tr>
<tr>
<td>VRAT (vertical recess array transistor)</td>
<td>see vertical channel NAND</td>
</tr>
<tr>
<td>VSAT vertical. see vertical channel</td>
<td></td>
</tr>
<tr>
<td>(V_{th}). see threshold voltage</td>
<td></td>
</tr>
<tr>
<td>(\Delta V_{th}). see Threshold Voltage Shift/Window</td>
<td></td>
</tr>
<tr>
<td><strong>W</strong></td>
<td>wrapped floating gate, 122</td>
</tr>
<tr>
<td><strong>Z</strong></td>
<td>Z-disturb, 184–185</td>
</tr>
<tr>
<td>Z-VRAT (zigzag vertical recess array transistor). see vertical channel NAND</td>
<td></td>
</tr>
</tbody>
</table>