Index

acceptance
  customer, 21
  product, 84
  quality team, 46
  reliability, 46, 88

air discharge
  cable discharge, 86–7
  charged device model, 15
  magnetic recording devices, 133–4
  micro-engines, 178
  micro-motors, 178
  paschen curve, 12, 170, 171, 178
  photo masks, 163, 168–73, 175, 177, 178, 180, 189, 190
  reticles, 168–73
  Toepfer’s law, 13, 135

air ionization
  contamination, 140
  ionizers, 29, 30
  negative charge ionizers, 141
  nuclear ionizers, 14
  photomasks, 168–73
  positive charge ionizers, 141
  reticles, 168–73

antistatic
  materials, 8–9
  topical, 8

applications
  automotive, 43–4
  cell phone, 72
  digital cameras, 75
  disk drives, 74
  hand held devices, 71
  laptops, 74
  servers, 73
  architecture
    DRAM, 31
    floorplanning, 105–9, 129, 147, 148
    I/O, 106
    image processing semiconductor chips, 75
    layout, 98, 100, 101, 105, 119, 120, 147
    microprocessors, 21
    mixed signal, 147–9
    mixed voltage, 148–9
    peripheral I/O, 106
    assemblies
      boards, 70–71
      cards, 70–71
      systems, 51
  auditing
    assembly, 33
    audit cycle, 33
    checklists, 22, 27
    documentation, 33
    ESD control program, 22
    factory, 32, 33
    manufacturing, 31
    reports, 28
    S20.20, 33
  avalanche
    avalanche breakdown, 13–15, 122, 170
    avalanche multiplication, 14, 134
bipolar transistors
- silicon, 184, 185
- silicon germanium, 156, 186
- parasitic bipolar transistors, 125
boots
- conductive, 28
breakdown
- air breakdown, 15, 133, 134, 137, 169, 190
- avalanche, 13–15, 122, 170
- devices, 126
- dielectric, 9
- semiconductors, 13, 14
bus
- bus resistance, 107, 110
- ground bus, 108–9
- power bus, 107, 108, 110, 150
cable discharge event (CDE)
- ESD networks, 16, 65, 83
- latchup, 88, 89
- pulse waveform, 85, 89, 90
- waveform, 89, 90
charge
- dissipative, 8, 81
- generation, 9
- static, 1, 9, 29, 144, 167, 169, 189, 190
- triboelectric, 22
charged board model
- test, 83
- verification, 86–7
- waveform, 86
charged device model (CDM)
- characterization method, 46
- ESD signal pin protection networks, 101
- failure criteria, 67
- failure mechanisms, 15
checklists
- audits, 22
- ESD protection design, 16
- manufacturing audit, 22
- semiconductor chip architecture, 109
- semiconductor chip design audit, 40, 58
- semiconductor chip design rule checking (DRC), 58
coordinators
costs
- factory, 167
- manufacturing, 167
materials, 167
nonconformance, 33
semiconductor chip area, 133
semiconductor chip performance, 121
criteria
- acceptance, 84
- qualification, 46
- standards, 22, 27, 28, 33, 40
degradation
- alternating current (a.c.), 26
- direct current (d.c.), 26, 71
- leakage, 68, 117, 142, 177
- radio frequency (RF), 117, 122, 123, 126
design synthesis
- ESD power clamp, 151–2
- ESD signal pin, 98
- ground bus, 108–9
- ground power rail, 97
- power rail, 97, 98
devices
- bipolar, 14, 122
- CMOS, 53, 56–8, 75, 89, 110, 123, 148, 184, 189
- gallium arsenide, 126
- MOSFETs, 58, 102, 184
- power MOSFETs, 9, 14, 41, 103, 105, 122, 184, 185, 187
- silicon germanium, 136
- silicon on insulator (SOI), 82
- silicon, 168, 190
dielectrics
- buried oxide (BOX), 9, 81
- inter-level dielectric (ILD), 9, 24, 120
- low-k, 184
- metal-insulator-metal, 120, 123
- thin oxide, 107
diodes
- ESD signal pin networks, 102, 106
- layout, 98–9
- series resistance, 138
dissipation
- charge, 8, 9
- current, 9
dissipative materials
- ESD bags, 31
- floor mats, 28–9
- mats, 27, 29, 32, 130
- table top, 70
electrical overstress (EOS)  
high voltage electronics, 78  
latchup, 65, 80, 189  
power electronics, 40  
electromagnetic compatibility (EMC)  
components, 16  
scanning sytems, 127, 161–3  
susceptibility, 41, 127, 160  
systems, 127, 163  
electromagnetic interference (EMI)  
equipment, 16  
noise, 16, 31, 78  
shielding, 84  
electromagnetic pulse (EMP)  
equipment, 50, 52  
noise, 71  
shielding, 57, 71  
electrostatics, 1–6, 11, 17, 21, 188  
charge transfer, 4, 10, 22  
charge, 169  
Coulomb’s law, 9  
current, 10, 15, 28, 48, 56, 69, 70, 77, 92, 97, 98, 99, 101, 118, 130, 141, 150, 171, 165, 187, 188  
electromagnetic compatibility (EMC), 16  
electromagnetic interference (EMI), 16  
field-induced charging, 88, 141  
fields, 176  
potentials, 80  
tri-bo-electric charging, 3, 7, 31, 88, 141  
electrostatic discharge (ESD) design  
floorplanning, 105–9  
placement, 109  
power clamps, 14, 56, 98, 103, 104, 107, 108, 110, 121, 123–7, 148, 149, 151  
rail-to-rail designs, 111  
signal pin designs, 110, 111, 112  
electrostatic discharge (ESD) power clamps  
bipolar, 103, 104, 123  
CMOS, 53, 57, 58, 88, 113, 122, 133, 167, 184  
electrostatic discharge program  
manager  
audits, 22, 24, 33  
checklists, 22, 27–30, 58  
committees, 33  
controls, 22  
handling, 131  
manufacturing, 33  
packaging, 31  
semiconductor chip design, 40, 58, 97, 107  
shipping, 31  
electrostatic discharge protected area (EPA), 22, 24  
equipment  
antistatic, 8  
auditing, 22, 24, 33  
automated, 43  
conveyor belts, 21  
dicing saws, 23, 24, 32  
ESD guns, 13, 83–6, 92, 155, 156, 161  
ESD semiconductor chip test equipment, 40  
ESD system test equipment, 83, 121  
handlers, 23–5  
problems, 23  
qualification, 46  
test equipment, 22, 24–7, 43, 48  
transmission line pulse (TLP) test equipment, 16, 41, 46–9, 168, 178  
facilities  
audits, 33  
controls, 21, 74  
coordinator, 32  
qualification, 46, 57  
tests, 24–7  
failure  
charged device model, 46  
conductor, 9  
device, 9, 39  
dielectric, 9  
human body model (HBM), 24, 67, 117  
human metal model (HMM), 83, 85  
IEC 61000-4-2, 83, 150  
machine model (MM), 117  
system, 71, 160  
failure criteria  
analog circuit, 104, 113  
digital circuit, 57, 147  
radio frequency circuits, 117  
feedback  
average multiplication, 14, 134  
regenerative feedback, 13  
floors, 28–9
floorplanning
  application specific integrated circuits (ASICs), 46
  charged device model ESD networks, 16, 41, 107
  DRAM, 31
  ESD signal pins, 101–2
  ESD power clamps, 108
  microprocessors, 21
footwear
  conductive, 26, 27
  dissipative, 28
  straps, 28

garments, 5, 23–5, 28, 29
grounding
  equipment, 25, 27
  personnel, 23, 25, 29
  surfaces, 27
  techniques, 29–30

guard rings
  ESD, 120
  ESD-to-I/O, 65
  I/O-to-Core, 89
  I/O to I/O, 89
  latchup, 58

human body model (HBM)
  characterization method, 41
  ESD power clamps, 98, 103
  ESD protection circuit solutions, 69, 97, 101, 102
  failure criteria, 66, 67, 152, 158
human metal model (HMM)
  air discharge method, 86
  characterization method, 83
humidity
  air discharge, 86
  relative humidity, 11

improvements
  continuous improvement, 33
  ESD manufacturing control, 1, 17, 22, 24, 25, 33, 34, 67
  ESD product roadmap, 25
  ESD product robustness improvements, 67, 78, 105, 133, 152, 155, 184, 187, 188
  yield, 21, 145

induction
  charging, 10, 88, 141
  static, 141
international electro-technical commission (IEC) 61000-4-2
  IEC bus, 150, 151
  power bus design, 151
  standards, 83
  technical reports, 22, 28
  technical specifications, 66, 150
inspections
  audits, 33
  corporate, 22, 32
  documents, 33
latchup
  characterization method, 42
  standard, 58, 59
  testing, 58
leakage mechanisms, 117
machine model
  ESD power clamp networks, 103
  ESD signal pin networks, 102, 106
  specification, 137
  waveform, 45
manufacturing
  air ionization, 29
  carts, 30
  equi-potential bonding, 27
  garments, 29
  shoes, 28
  wrist straps, 28
materials
  conductive, 26, 27, 143
  dissipative, 8–9
  packaging, 31
  protective, 32
  shielding, 71
mats
  conductive, 27
  dissipative, 8–9
  flooring, 28, 29
meters
  field meters, 27
  ion current, 15
Index

monitors
charge plate, 26, 27
models
cable discharge event (CDE), 16, 40, 66, 87–9, 141, 142
cassette model, 41, 45–6
charged board model (CBM), 83, 86–8
charged device model (CDM), 10, 13, 15, 16, 41, 46, 67, 70, 98, 107, 137, 179
human body model (HBM), 5, 16, 22, 41–3, 67, 98, 103, 117, 135, 137, 175
human metal model (HMM), 16, 40, 66, 68, 83–7, 150, 161
IEC 61000-4-2, 40, 66, 68, 74, 83, 93, 149–52, 161
latchup, 58
machine model (MM), 13, 16, 41, 43–5, 67, 98, 117, 137, 178
transient latchup, 58
transmission line pulse (TLP) model, 41, 46–50
very-fast transmission line pulse (VF-TLP) model, 41, 136
MOSFET
avalanche breakdown and snapback, 13–15
nano-structures
carbon nano-tubes (CNT), 187–8
carbon nano-wires, 188
FinFETs, 163, 168, 185–7
micro electro-mechanical (MEM), 168, 176–7, 180, 182
micro-mirrors, 163, 176, 182, 183
micro-motors, 163, 178–81
noise
latchup and noise, 58
off-chip ESD protection
board level ESD protection, 144
conductive polymers, 127, 163
on-board diode components, 133
transient voltage surge (TVS) protection, 141
packaging
materials, 31
procedures
manufacturing, 21–34
semiconductor chip design, 40, 58, 97, 107
system level, 74
qualification
manufacturing line, 22, 23
product, 46
technology, 46
safe area, 27, 28
safe operation area (SOA)
electrical safe operation area (E-SOA), 122
thermal safe operation area (T-SOA), 122
transient safe operation area, 55
shielding
electronics, 71
materials, 9
packaging, 8, 31
systems, 71
shipping trays, 32
shipping tubes, 31, 51
shunts, 97, 100, 103, 118, 120, 121, 143, 145, 146
silicon controlled rectifiers, 58, 101
standards
JEDEC latchup standard, 156
system level testing
cable discharge event (CDE), 65, 66, 68, 83, 87–92
ESD gun, 83–6, 92
human metal model (HMM), 66, 83–7
IEC 61000-4-2, 66, 74, 83, 93
radio frequency (RF) testing
methodology, 117
test
capacitive probe, 88, 116, 118, 120
ESD, 25–34, 39, 44, 46, 68, 83, 158, 160, 182
equipment, 23–7
facility, 30, 33
garments, 23, 29
laboratory, 3, 11, 80
latchup characterization, 41, 58, 59
shipping tubes, 31, 51
table top, 70
tape-and-reel, 21
trays, 27, 30, 32, 51
wrist straps, 23, 28, 29, 88
test techniques
  chip level, 98, 121, 142, 147
  product level, 53, 54
  system level, 65–7
transmission line pulse (TLP) testing
  I-V characteristic, 186
  standard practice, 33, 40, 47, 112–14
  standard test method, 28–31
  system configurations, 46, 85

trays, 27, 30, 32, 51
tribocharging, 23, 28
voltmeters, 27, 28, 30
work positions, 178, 180
work surfaces, 22, 25, 27, 29, 31
wrist straps, 23, 25, 28, 29, 88
yield, 1, 21, 34, 57, 145, 172, 189