Index

Address Space
Models 36
Mapping PCI 138
Mapping Process 154–155
Alignment, Data 47
Applications
  DSP interconnect 227–234
  I/O interconnect 9, 29, 35, 250–251
  Mezzanine interconnect 288, 290, 293–295
  Processor interconnect 1–3, 8, 24–26, 27–29
  ATM (interoperability) 209, 218–219
Atomic Operations 36–27, 45
Board Routing 133–134
Boot Requirements 153
Bringup, System 62, 179–182
Bus Loading (Traditional buses) 6
Byte Lane and Byte Enable Usage 47–48, 149
Canceling Packets 94
Cellular, see Wireless Infrastructure
Channel Characteristics, Electrical 288
Class of Service 204, 210
Clocking Requirements 131–132, 249, 269–270
Code-Groups 79–84
Command and Status Registers (CSRs) 45
Configuration, Device 45–46, 156–182, 260
Congestion Detection 184–187
Control Symbols
  Corruption 99
  End-of-packet 75
  Generator 257
Link-request 76, 112
Link-response 73, 113
Multicast-event 76, 197
Packet-accepted 71, 110
Packet-not-accepted 73, 110
Packet-retry 72, 110
Protection 118
Transmission Alignment 83, 113–117, 254–255
Recovery 100–101
Restart-from-retry 75
Start-of-packet 75, 85
Status 73
Stomp 75
CRC Codes 16, 24, 41, 69–70
CSIX 211–216
Data Streaming Logical Layer 199–209
Deadlock, Avoidance 33, 96–98
Destination IDs 64, 194–195
Device Access Routine (DAR) Functions 173–179
Discovery 23, 61–62, 153, 179–182
Doorbell Operations 17–18, 50–51
8B/10B Coding 21, 77–84
Elasticity Mechanisms 132
Enumeration 10
Error
  Coverage 23, 69, 119, 264–266
  Detection and Recovery 23, 98–102, 264–266
  Handling 98–99, 190–191, 264–266
  Lost Packet 23, 98, 208–209
  Management 23, 183, 187–189
  Non-recoverable 265
Ethernet 9, 11, 217
Fault Tolerance see Error Management
Fibre Channel 8
Flow Control 89
End to End 184–187
Received Controlled 89
Transmitter Controlled 92
FPGA Technology 279–285
Globally Shared Memory 191–194
HAL Functions 154–182
Hardware Inter-operability Platform (HIP) 291
Hot Swap 188
I/O Logical Operations 35–48, 247
Idle Control Symbols 84, 87, 101
Initialization, see Bringup
Input-status, command 8.7
Interrupts 2.6, 5.1.5.2, 14.3.6
Link
Initialization 128
Maintenance Protocol 94, 119
Protocol Violations 101–102
Training 128–129
Mailbox Structures 54–59
Maintenance
Operations 45–46, 119–121, 126–128
Routing Packets 65
Training 128–130
Mechanical Environments
Advanced Mezzanine Card Serial RapidIO (PICMG AMC) 293
Advanced Module Format (VITA 46) 295
AdvancedTCA Serial RapidIO (PICMG 3.5) 292
CompactPCI Serial RapidIO (PICMG 2.18) 291
Switched Mezzanine Card XMC (VITA 42) 293
VME Switched Serial VXs for RapidIO (VITA 41.2) 294
Memory Coherency, see Globally Shared Memory
Message Passing Operations 17–18, 51–53
Multicast Packets 194–196
Multicast Symbols 197–198
Multiprocessing, see Globally Shared Memory
Ordering Rules 30–33
Output Retry-Stopped 93
Packet
Alignment 124–125
Buffers 272
Exchange Protocol 85–86, 116
Format 16
Overhead 25
Pacing 123
Priority 68, 96–97, 117–118, 275
Protection 69–70, 119
Termination 122
PCI, PCI-X, PCI Express
Interoperability 137
to RapidIO Transaction Flow 139–143
Ordering Considerations 145–146
Problems with 7
PCS Layer 21, 78
Performance Monitoring 14.3.4
PMA Layer 22, 79
Port
Initialization 85, 126–127
Width Mode Selection 126
Mirroring 275–276
Port Write, Command 45–46, 189, 262
Read Operation 39
Reset 190
Response Packet Formats 16, 37–39
Retimers and Repeaters 103
Retransmit queue 118
Routing look-up 277–278
Routing Tables 64, 277
Running Disparity 81
Segmentation and Reassembly 206–209
Segmentation Contexts 207
Signal Skew 6, 89, 133–134
Source Routing 25
Streaming Write 44
Switch
Features 271–273
Flow Control Rules 187
Packet Priority 275
Symbol see Control Symbol
System Level Addressing 6
TCP Offload 218
Termination, Electrical 21, 133, 135,
Topology, System 62–63, 229–235
Traffic Management 210
Training Pattern 129
Virtual Streams 204
Virtual Queues 204
Wireless Infrastructure 226–235
Write Operation 42–43