Index

References to figures are given in italic type. References to tables are given in bold type.

3D transistors, 342
absolute maximum ratings (AMR), 164, 301, 303
advanced controls, 16, 19
advanced design system (ADS), 96–7
air discharge see indirect discharge
aircraft, 61, 239
AMR (absolute maximum rating), 164, 301, 307
Android debug bridge (ADB), 204
ANSI/ESD SP5.6–2009, 62
antifragile systems, 357–8
application specific integrated circuit
(ASIC), 369–75, 380, 385
approved vendor list (AVL), 381
Arduino, 176
audio interfaces, 259–60, 260, 314
automated scanning, 68, 69
automatic error correction, 172
automatic test equipment (ATE), 226, 297, 331
automotive industry, 33, 48
body damage, 361–3, 361, 362
communication bus systems, 299–302
see also controller area network;
FlexRay; local interconnect network
control systems, 313
ground loss, 317
inductive load switching, 130–1
keyless entry systems, 311–13
load dump, 315–17
on-board and internal ESD protection, 324–9
ground shift due to system ESD, 325–6
lateral coupling, 326–7
on-chip ESD protection optimization, 324–5
operating voltages, 315, 329
pre-pulse voltage, 320–1
PCB layout, 328–9
power supplies, 303
protection design window, 324
requirement for high ESD levels, 294–9
return rates
due to ESD events, 296–7
due to incomplete specification, 297–9
reverse polarity, 318–19
safe operating area checks, 330, 331
sensors and sensor interfaces, 304–6
soft errors, 176
standards, 58–60, 78
transient voltage suppressors (TVS), 315, 322–3
verification and qualification, 329–32
ESD design rule check, 330
average selling price (ASP), 371
avionics, 61

ball grid array (BGA) substrates, 369, 371
basic control, 16, 19
bill of materials (BOM) cost, 359, 367, 370, 371–2
bit error rate (BER), 123
black swan events, 357
black-box systems, 203
blue screen of death (BSOD), 365
bulk current injection (BCI), 323
bypass capacitor, 88

cable discharge event (CDE), 4, 34–5, 82–3
mobile devices, 248
shielded cables, 65
testing, 63–7
transmission line pulsers (TLP), 66–7
unshielded cables, 65–6
cameras
in device, 126, 204–5, 209, 264, 359
for failure recording, 181
CAN see controller area network
capacitors, 161–2
bypass, 88, 154
decoupling, 94, 303, 307–9, 312, 319
ESD pulse generation, 50–1, 91
fast transient behavior, 106, 108
local injection via, 193–4, 196
low-pass filter, 249–50, 261, 281
cases, 131, 356
mobile devices, 262–3
Cat 5 cable, 63–5

CCE see cable discharge events
cell phones, 176–7, 177, 178
clamshell type, 266
face-down on table, 263–4
see also mobile devices
central office (CO), 373
central processing unit (CPU)
error logs, 205
physical damage, 367
susceptibility scanning, 188
system clock, 207–8, 211
USB data transfer rate, 346

charge coupled transmission line pulse (CCTLP), 92
charged board event (CBE), 5, 15, 82, 83
charged cable events see cable discharge events
charged device model (CDM), 2, 17
automotive industry, 298
model correlations, 36
pulse magnitude, 4
technology roadmap, 21
test protocol, 18
charging cables, 234, 263–4
Chelyabinsk Meteor, 364
chip ferrite bead (CFB), 87, 88, 89, 105–6, 159, 274, 275, 279, 344
circuit simulation, 102–4, 103
clock disturbance, 207–12
CMF see common mode choke/filter
co-design, 85–6, 359, 359–61
definition, 1
margin requirements, 360–1
long tail events, 363–4
combinatorial circuits, 202–3
commercial off-the-shelf (COTS) parts, 369
common mode choke/filter (CMC/CMF), 88, 162–3, 300–1, 300, 343
complementary metal oxide semiconductor (CMOS), 42, 88, 110, 129–30, 346
component level ESD, 2–3, 3
component tests, 17–18
end-user ESD, 353–4
contact discharge see direct discharge
contract manufacturers (CM), 358, 365
central office network (CAN), 33–4, 131, 137, 301
common mode chokes on, 300–2
ground loss, 317
load dump, 316
cost allocation, 354–5, 358, 359–60
bill of materials (BOM) cost, 359, 367, 370, 371–2
components, 369
cost competition, 372
performance, 370–1
enhancement, 372–4
production cost, 371–2
profit margin, 370
time-to-market, 375–6
user experience, 366–7
CRC see cyclic redundancy check
cross-coupling, 20, 119, 176, 339
crosstalk reduction, 219–20
cumulative distribution function (CDF), 355
current diversion, 216, 217
current force probes, 118
current limiters, 132, 134–5
current spreading reconstruction, 190, 191, 192
customer premises equipment (CPE), 373
customer return costs, 367–9
cyclic redundancy check (CRC) errors, 203, 214, 216
dashcams, 365
decision theory, 355
dielectric breakdown, 36
diode-triggered ESD protection, 322
diodes, 134, 153–4, 322
simulation, 104–5
see also light-emitting diodes; transient voltage suppression; Zener diodes
direct discharge, 3, 25–6, 54–5
soft failure, 226
direct power injection (DPI), 319, 320
directional injection, 198
discharge path
between devices, 248
mobile devices, 244
through external interface, 258–9
through housing, 262–3
through speaker interface, 260–2
simulation, 98–116
display interfaces, 288
see also liquid crystal display
Display Port, 346
distant error, 176, 340–1
double data rate (DDR), 342
DSP chip, 371–2
electric field probes, 185
electrical overstress (EOS), 4, 5, 15, 89, 297, 298, 332
distinguished from ESD, 15, 39
physical damage, 361, 362, 365, 383
Electromagnetic Compatibility (EMC) Directive (EU), 47
electromagnetic radiation, 339
electronic design automation (EDA), 103–4
emission microscopy (EMMI), 42
emulator see simulator
derail of line (EOL) test, 294
entertainment systems, 314
error-detecting codes, 202–3
escalation strategy, 181–2
ESD gun, 34, 37
ESD protected areas (EPAs), 16–17, 365
Ethernet cable, 63–4, 82–3
European Union standards, 47–8
eye diagram, 135
failure
hard see hard failure
soft see soft failure
failure analysis (FA), 353, 367–9
fast Fourier transform (FFT), 211–12
fast-ESD, 249–50
ferrite beads, 87, 105–6, 159, 273, 274–5, 279, 344
FinFET, 342
firmware, 117, 123, 218, 336
flash memory, 215
FlexRay bus, 301, 303
load dump, 316
functional latch-up, 121, 121
galvanic isolation, 313
gas discharge tubes (GDT), 134, 156–8, 373
gate coupled NMOS (GCNMOS), 78, 322
gate oxide damage, 129–30
general purpose IO (GPIO), 176, 347
global pin, 182
graphic processing unit (GPU), 380
ground connection
mobile devices, 234–9, 280–2
impedance effect, 283, 283
PCBs, 32
ground (continued)
  loss, 244, 317
  return path, 25, 85, 99–100, 185, 235, 337
  see also discharge path
  ground impedance effect, 283
  grounded gate n-channel MOS (GGNMOS), 78
  grounding clips, 264–5

  hard failure, 3
    characterization, 97–8
    IEC testing, 42
    test results evaluation, 67
  HDMI, 89
    capacitance thresholds, 135
    design challenges, 344–5
    USB and, 346
  headsets, 246–7
  high definition multimedia interface see HDMI
  high-speed serial (HSS) link IO, 18, 20
  high-speed systems, 342–5
  Hindenburg disaster, 354
  hinge interconnects, 265–6
  horizontal coupling plane (HCP), 32, 57
  hot plug-in, 300–1
  human body model (HBM), 2, 17
    automotive industry, 298, 323
    IEC tests and, 5, 6, 36, 37–41, 74–6
    on-chip systems, 74–6
    physical damage, 41, 43
    pulse magnitude, 4
    target levels, 20
    technology roadmap, 20
    test protocol, 17–18
    waveform shape, 75
  human metal model (HMM), 32, 33, 74–6
  pulse sources, 138
  humidity, 53, 54, 240

  IC package technologies, 347
  IC pins, 164
    classification
      class 1, 182
      class 2, 182
      class 3, 182
      class 4, 182
    direct injection into, 120
    dual diode protection, 108–10
    failure at unexposed, 327
    failure modes, 335
    failure thresholds, 124, 126
    ground, 308, 310, 317
    grouping, 227
    hard damage, 97–8
    HBM test, 18, 20, 37–41, 75–7
    isolation resistors, 87, 88
    layout, 328–9
    protection design window, 131
    reference clock, 211, 212
    residual pulse, 6–7, 85, 105, 115
    TVS devices, 90–1
    voltage clamps, 81, 82
  IC pins ground level bounce at, 251
  IEC 61000–4–2 test
    coupling planes, 57
    discharge methods, 22
    discharge network, 24
    environmental conditions, 53–4
    human body model tests and, 5, 6, 36, 37–41, 74–6
    ISO 10605:2008 and, 60–1, 60
    pulse waveform, 23, 24, 75, 248
      modeling, 26–8, 114–16
      reproducibility, 70–2
      rise time, 115
      reproducibility, 138
      soft failures, 224–5
    standards requirements, 49–58
      coupling planes, 56–7
      direct vs air discharge, 53–4
      ESD simulators, 50–2
      test results, 57–8
      test setup, 52–3
      subsystem and module testing, 56–7
      system configuration, 56
      test points, 55–6
      transient voltage suppressors, 137–8
  IEC 61000–4–5 test, 31–42
    ohmic pulse sources, 33–4
Index

printed circuit boards, 32–3
pulse waveforms, 31
IEC tests
correlation with HBM thresholds, 36, 36
future specification requirements, 350–1
TS 62228, 34
in-band errors, 174–5, 224–5
indirect discharge, 3, 25–6, 321
IEC 6100–2–4 standards compliance
and, 54–5
soft failure testing and, 179
induced electric fields, 255–7
Industry Council on ESD Target Levels
      JEP161, 5, 116, 342
      JEP155, 44, 333, 352, 388
      JEP157, 44, 352, 388
      JEP162, 13, 127
      Whitepaper III, 371
input/output buffer information specification (IBIS), 104, 198, 224, 276
inter-modulation distortion (IMD), 274
International Electrotechnical Commission (IEC), 3
International Organization for Standardization (ISO), 48
IO cells
      failure signatures, 111–12
      high current conditions, 110
two-diode protection, 106–12
ISO 7637–2, 315
ISO 10605:2008, 29, 58–60, 60, 249, 312
tabletop setup, 30
test parameters, 30
ISO 90610:2008, 78
isolation resistor, 88, 91

Joint Electronic Devices Engineering Council (JEDEC), 17
K-line, 302
kernel debugging, 204–5
key mats, 252–3, 255
latch-up, 121, 121, 257, 332, 338–9
testing, 172
lateral coupling, 326–8
leakage current, 320–1
light-emitting diodes (LED), 298
keyless entry systems, 311–13
lighting, 313–14
optical ground isolation using, 177
lightning damage, 130, 363
liquid crystal display (LCD), 179
flex cable, 223
stripe errors, 209, 210–11, 210
susceptibility scanning, 187, 188–9
load dump, 315–17
local error, 176
local injection, 191–201, 196, 196
directional, 197–201
via capacitor, 193–4, 196, 196
via diode, 194–5, 196, 196
via resistor, 193
local interconnect network (LIN), 33, 34,
      137, 302–3
load dump, 316
local pin, 182
long tail events, 363–4
low dropout (LDO) voltage regulator, 303
low-pass filtering, 217
machine gun timing problem, 355
machine model (MM), 17
magnetic field probes, 186
Maxwell solvers, 101–2, 103
medical applications, standards, 60–1
medical equipment, 60–1
memory boards, 56
memory errors, 366
memory interfaces, 289–90
metal oxide varistors (MOV), 10, 105, 134,
      143, 154–5, 162
microelectromechanical system (MEMS),
      305–6, 348
microvaristor, 154
microwave oven, 236, 237
military applications, standards
      requirements, 60–2
mobile devices
      cable interface design, 269–80
      cable placement, 269–71, 274–5
mobile devices (continued)
floating device, 235
interface with ferrite rings, 279
interface guiding noise to cables, 276–8
interface with high impedance on each input, 278–80
noise current localization, 274–5
protection components, 275–80
TVS directionality, 271–3
charge generation example, 246–7
common mode current path, 269–71
critical internal interfaces, 289–90
delicate sensors, 289
design principles
grounding clips, 264–5
hinge interconnects, 265–6
discharge paths, 234–9, 244
human-mediated, 237–9
through external interface, 258–9
through housing, 262–3
ESD generation examples
accidental charge in grounded system, 240–4, 241
charge generated by person inside car, 240
floating metal object, 241–3
large machines, 239–40
measurement devices in grounded environment, 243–4
triboelectric series, 340
fast and slow pulses, 249–50
ground bounce, 250–2
insulator surface behavior, 244–5
discharge at, 245–6
isolation
induced electric fields, 255–7
key mat hole positioning, 255
solid glue, 253–4
via material thickness, 252–3
key mats, 252–3
orientation effects, 259–64
PCB layout, 267–9
board edges, 285–7
common mode impedance concerns, 280–7
isolating signals with shield grounded to internal layers, 282–3
protected interfaces, 288–9
pulse waveforms, 248
self-capacitance, 234–6
shielding, 257–9
software considerations, 287–91
delayed effects, 290–1
versions utilised, 291–2
stacked chips, 283–4
test methods, 248–9
unidirectional interfaces, 288
see also cell phones
Monte Carlo analysis, 357
multilayer flex, 266
navigation systems, 314
near-field (NF) scanning, 211
Nielsen surveys, 366
noise, 61, 174–5
attenuation, 88–9, 159–60, 183
common mode, 162
direct injection, 197–201, 215
ESD waveforms, 72, 138, 197
estimation, 225
PCB sensitivity, 183, 186, 188, 190
supply, 121
switching, 31
system clock, 207, 211
numerical solvers, 101–4
off-chip protection, 79–82
on-board diagnostics (OBD), 300
on-chip systems
compared to off-chip systems, 84
ESD protection, 74–8
Open Media Applications Platform (OMAP), 94, 94–7, 95, 96
optical interfaces, 348
out-of-band errors, 174–5, 225
over-specification, 298
packing materials, 14, 131
parasitic effect, 106, 261, 370
passive components, 87, 116, 161, 224, 301
Index

phase-lock loop (PLL) disturbance, 176, 204, 207–12, 213
photo frames, 204–7
physical damage, 129–30
protection, 130–3
pi networks, 133
pins see IC pins
plastics, 222
plugin cards, 56
polymer components, 134, 348–9
diodes, 105
polymer voltage suppressors (PVS), 155–6, 344, 357
power clamps, 112–14, 176
power supplies, 113–14, 130, 215, 303, 332
control systems, 313
see also charger cables
power-on self test (POST), 367
primary and secondary protection, 163–4
printed circuit boards (PCB)
board edges, 285–7
future challenges, 347–8
IC co-design, 82–4
IEC 61000–4–2 test, 32–3
mobile devices, 267–9, 285–7
models, 104–6
mounting holes, 286–7
panels, edge challenges, 287
spark gaps, 158–9
test traces, 286
probes, 184–6, 185, 186
product reliability testing, 48–9
profit margin, 370
programmable electrical rule check (PERC), 227
protection design window, 131, 324
pulse injection, 118–20
qualification testing, 3
relative humidity, 53, 54, 240
residual pulse, 6, 7, 78, 90–1, 90, 94, 96, 99
resistor-capacitor network (RC), 37
resistors, 161
discharge, 50
ground plane coupling, 52
isolation, 87, 88, 93
local injection via, 193, 194, 199
on-board, 82
physical damage, 222
reverse bias configuration, 143, 147, 149
ringing pulses, 176
risk analysis, 354–5
rotary encoders, 309
S-parameters, 135–7
safe operating area concept, 224–5, 225–6
automotive industry, 330
scanning electron microscopes (SEMs), 368
SCR see silicon controlled rectifier
SD cards, 215–16
secondary ESD, 179, 341
sensors, 304–10
metallic cover, 305–6
serial advanced technology attachment (SATA), 179
serializer/deserializer (SERDES) macros, 342
shielding
backside, 308, 310
cables, 65
ICs, 217–18
mobile devices, 257–9
signal integrity, 121
eye diagrams, 135–7, 136
soft failure and, 123–5, 224–5
silicon-controlled rectifier (SCR), 78, 81, 84, 98, 130, 134, 150–3, 323, 332
simulation (software)
IO cells, 106–12
limitations, 339–41
model types, 103–4
PCB devices, 104–6
power clamps, 112–14
failure thresholds, 113
SEED, 98–101
soft failure, 201–5, 227
tools, 101–4
see also charged device model; human body model; human metal model;
IEC 600042–2
simulators (electrostatic discharge), 26, 62–3, 70–2
simulators (electrostatic discharge) (continued)
SEED analysis and, 337–41
soft failure and, 223–4
standards requirements, 50
slow-ESD, 249–50
snapback, 88, 100, 105, 133, 151–2, 158, 315
soft failure, 3, 42–3, 169–70
amplified, 176–7
characterization, 116–20, 182–205
current spreading reconstruction, 190
local injection, 191–201
susceptibility scanning, 183–90
variables affecting, 171–2
countermeasures, 228
crosstalk reduction, 219–20
current diversion, 216, 217
current reduction by resistance, 220–2
design principles, 223–30
closure shield junction, 218
ESD avoidance, 222–3
filtering, 217
firmware methods, 218
secondary ESD avoidance, 218
shielding, 217–18
design strategy, 228
block-level simulation, 227
debugging, 228–9
ESD coupling grouping, 226–7
IC pin grouping, 227
safe operating area, 225–6
SEED simulation, 227
direct discharge, 226
escalation strategy, 181–2
examples
direct field coupling on USB bus, 212–14
field injection on DUT, 204–7
PLL disturbance measurement, 207–12
failure threshold, 179
indirect discharge, 226
IO cells, 109
latch-up, 121–3
local vs distant error, 176
mobile devices, 256–7
mode classification, 173
in-band/out of band with respect to pulse width, 175–6
in-band/out of band with respect to voltage, 174–5
out-of-band errors, 225
pin-specific, 120–3
self-curing, 170
signal integrity problems, 123–5
software analysis, 201–5
black-box type systems, 203
kernel debugging, 204–5
register monitoring, 203–4
spectral analysis, 211–12, 212
system level tests, 178–82
test optimization, 179–82
test results evaluation, 67
USB, 345–6
user sensitivity, 170
sousveillance, 364–5
spark gaps, 158–9
sparking, 220–2, 222–3
speakers, discharge through, 260–2
spectrographic analysis, 211–12, 212
SPICE models, 6–7, 91–4, 102, 103, 201, 224, 334–5, 339
stacked chips, 283–5
standards compliance
ANSI/ESD SP5.6–2009, 62–3
automotive industry, 58–60
legal, 47–8
medicinal, 60–1
military, 61–2
test result evaluation, 67
root cause determination, 67–70
stress models, 17
charged device see charged device model
human body see human body model
machine see machine model
supply noise, 121
surface acoustic wave filters (SAW), 41, 114, 341
surface mount device (SMD), 41, 88, 154, 159, 162
surface mount technology (SMT), 347
8/20us pulse (IEC61000-4-5) see also lightning damage,
surge protection devices (SPD)
gas discharge tubes (GDT), 134, 156–8, 373
thyristor, 159
transient voltage suppressor diode see transient voltage suppression
susceptibility scanning, 181, 183–90, 228
comparative, 188
equipment, 183–4, 184
example results, 186–9
probes, 184–6
test levels, 189–90
System Level Electrostatic Discarge (ESD) Simulator Verification Standard Practice, 71
system level tests, 21–9
component level testing and, 37–41
correlation studies, 41–2
ESD simulators, 26
grounding condition, 25
objectives, 47
reproducibility, 70–2
root cause determination, 68–71
soft failure, 178–82
waveform modeling, 26–8, 337–8
measurement, 71–2
reproducibility, 70–2
system-efficient ESD design (SEED), 46, 84–9, 86
automotive industry, 306, 314, 323
verification, 329–32
basic simulations, 91–4
design methods, 90–1
discharge path simulation, 98–116
harmonized approach to system protection, 349–51
model refinement, 334–5
roadmap for expansion, 335–7
comprehensive design verification, 341–2
soft failure prevention, 227
USB interfaces, 94–7
system-in-package (SiP), 347
systems on chip (SoC), 296, 347

Taleb, Nicholas, 356, 357
television sets, 14
test traces, 286
testing, system level see system level tests
thermally induced voltage alteration (TIVA), 42
thyristor surge protection devices (TSPD), 159
time domain reflectometry (TDR), 374
toasters, 236
trace grouping, 226–7
trace resistance, 88
transient behaviour
fast transients, 88, 106, 135
robustness, 319–20
transient latch-up (TLU), 4, 121, 122, 127, 176
transient voltage suppressor (TVS), 6–8, 16–17, 79, 88, 133
automotive industry, 315, 322–3
bidirectional, 134, 271–3
characterization
screen shots, 138
transmission line pulse, 139–41
choice, 164–6
coordination between device and nodes, 165–6
IEC 61000–4–2 test, 137–8
mobile devices, 271–3, 279–80
off-state properties, 135–7
polymer-based, 348–9
snapback, 133–4
spark gaps on PCBs, 158–9
to inject ESD pulse, 117–19
transient behavior, 105
ultralow capacitance, 151–2, 279–80
unidirectional, 134, 271
voltage clamping, 133–4, 271
transmission line pulse (TLP), 33, 41–2, 66–7, 74–5, 139–41, 317
as approximation to IEC waveform, 78
transmission line pulse (TLP) (continued)
  automotive industry, 331
  charge-coupled (CCTLP), 92–3
  correlation issues, 78
  I-V characteristics, 77
  IC pin evaluation, 164
  on-chip systems, characterization, 76
  represented as series diodes, 92–3
  SEED simulation, 91–3
  system schematic, 77
  triboelectric charge, 240, 240, 246–7
  troubleshooting, 68

un-assembled components, 2–3
uncertainty, 354–5
Universal Serial Bus see USB
USB, 8, 89
  3.0, 123, 345–6
  cables, 63
  capacitance thresholds, 135, 370
  common mode filter, 87–90
  connector junction, 218, 314
  current spreading reconstruction, 190
  data bus soft failure, 212–14
  design challenges, 343–5
  hard failure, 387
  HDMI and, 346
  IO cells, 111
  soft failure characterization, 116, 122, 123, 197–8, 204

system-efficient ESD design (SEED), 94–7
user experience, 366–7
  customer return costs, 367–9
  quantification, 367
users, extreme and abusive, 361–3

varistors, 105
  ESD generation by person inside, 240, 241
  ESD generation and mobile devices, 239–40

  see also automotive industry
  vertical coupling plane (VCP), 25, 29, 53, 57
  very fast transmission line pulse (VFTLP), 9, 33, 75, 78, 92, 111
  voltage limiters see transient voltage suppressors
  voltage regulators, 332

  watchdog timers, 203
  Wunsch-Bell relation, 39–40, 39

X-by-wire, 304–5, 313
Zener diodes, 82, 82, 134, 143 50
  leakage, 149–50
  reverse bias configuration, 143, 147, 149
  state transition time, 145