## CONTENTS

Preface vii

1 Introduction 1
   1.1 Power Supply Noise 2
   1.2 Power Network Modeling 4
   1.3 Modelling of Switching Currents 12
   1.4 On-Chip Decoupling Capacitance 16
   1.5 On-Chip Inductance 20
   1.6 Process Scaling Impacts 28
   1.7 Summary 32

2 Design Perspectives 33
   2.1 Planning for Communication Chips 34
   2.2 Planning for Microprocessor Chips 44
   2.3 IBM CAD Methodology 55
   2.4 Design for IR Drop 62
   2.5 Package-Level Methodology 67
   2.6 Summary 73

3 Electromigration 75
   3.1 Basic Definitions and EM Rules 75
   3.2 EM Analysis Tool 80
   3.3 Full-Chip EM Methodology 83
   3.4 Summary 85
4 IR Voltage Drop
  4.1 Causes of IR Drop 87
  4.2 Overview of IR Analysis 89
  4.3 Static Analysis Approach 96
  4.4 Dynamic Analysis Approach 99
  4.5 Circuit Analysis with IR Drop Impacts 103
  4.6 Summary 103

5 Power Grid Analysis 105
  5.1 Introduction 106
  5.2 Executing the Tool 108
  5.3 Advanced Static Analysis 119
  5.4 Dynamic Analysis 125
  5.5 Layout Exploration 129
  5.6 Summary 133

6 Microprocessor Design Examples 135
  6.1 Intel IA-32 Pentium-III 135
  6.2 Sun UltraSPARC 139
  6.3 Hitachi SuperH Microprocessor 141
  6.4 IBM S/390 Microprocessor 146
  6.5 Sun SPARC 64b Microprocessor 148
  6.6 Intel IA-64 Microprocessor 153
  6.7 Summary 156

7 Package and I/O Design for Power Delivery 157
  7.1 Flip-Chip Package 157
  7.2 Simultaneous Switching Noise (SSN) 159
  7.3 Case Study of a Microprocessor-Like Chip 167
  7.4 Power Supply Measurement 181
  7.5 I/O Pads for Power/Ground Supplies 188

Glossary 191

References 199

Index 205