Chapter 1

Amplification in Linear Mode

1.1. Principles of microwave amplification

An amplifier is a device used to convert some of the power supplied by a direct current (DC) signal from a continuous power source into alternating current (AC) power at the frequency of the microwave signal applied on the input. It consists of the following elements:

– active components used for the amplification of the signal, such as bipolar (HBTs, etc.) and field-effect (MESFETs, HEMTs, etc.) transistors;

– passive components used for the polarization and impedance matching networks, such as transmission line segments, resistors, inductors and capacitors.

![Figure 1.1. Principle of amplification](image)

It is possible to essentially classify microwave amplifiers according to various criteria, although this list is not exhaustive:

Chater written by Jean-Luc GAUTIER and Sébastien QUINTANEL.
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– Output power:
  - low power: output power of a few tens of mW, operating in linear mode;
  - medium power: output power ranging from a few hundred mW to a few W, essentially operating in nonlinear mode;
  - high power: output power greater than a few W, operating in nonlinear mode, taking the phenomena of power dissipation into account.

– Frequency band of operation:
  - narrowband: relative bandwidth $\frac{\Delta f}{f_0}$ a percentage of several tens %;
  - wideband: $\frac{f_{\text{max}}}{f_{\text{min}}}$ in the order of an octave;
  - ultra-wideband: $\frac{f_{\text{max}}}{f_{\text{min}}}$ in the order of a decade.

– Noise factor.

1.1.1. Characteristics of an amplifier in linear mode

The linear dynamic operation of an amplifier can be represented by the circuit diagram shown in Figure 1.2.

![Figure 1.2. Diagram of the linear amplifier principle](image)

The impedance value of the generator and the load is standardized and generally equal to 50 $\Omega$.

The essential characteristic values of an amplifier are:

– Power gain: the most commonly used parameter is transducer power gain, which is expressed in dB and defined as the ratio of dissipated power in the load and the power available at the generator terminals. This value is often supplemented by the gain ripple in the bandwidth.
\[ G_0 \pm \Delta G \text{ in } dB \]

– The input and output impedances, generally represented by their reflection coefficients normalized in relation to 50 Ω.

The port reflection coefficient is usually expressed in dB and sometimes as a standing wave ratio (SWR).

\[
|\Gamma_{Ei}|_{dB} = 20 \log |\Gamma_{Ei}|
\]

\[
SWR_i = \frac{1+|\Gamma_{Ei}|}{1-|\Gamma_{Ei}|} \text{ with } i = 1.2
\]

– The frequency band of operation, which is usually limited by the conditions for impedance matching, i.e. the frequency band in which the port reflection coefficient is less than a given value, for example, –15 dB. This frequency band is either characterized by a relative value that is normalized to the central frequency \( f_0 \) and \( \Delta f \), or by the ratio between the maximum and minimum frequency

\[
[f_{\min}, f_{\max}] \text{ and } \frac{f_{\max}}{f_{\min}}.
\]

Figure 1.3 shows the gain and matching curves defining the circuit bandwidth.

![Transducer power gain and Input matching curves](image)

**Figure 1.3. Linear characteristics of an amplifier**

– The noise factor \( F \), which is expressed in dB, if it is included in the technical specifications. It determines the noise floor of the amplifier, expressed in dBm, which is the minimum input power such that the signal level is above the noise level:
Noise floor = \frac{N_s}{G} = N_E + kT_0 \Delta f (F - 1) = k (T_E + T_A) \Delta f

\Delta f : \text{Amplifier bandwidth}

T_E : \text{Equivalent noise temperature of input load}

T_A : \text{Additional noise temperature of amplifier}

The concepts of noise and noise temperature are discussed in section 1.1.2.

– The linearity of the amplifier characterized by maximum input or output power to ensure linear operation of the amplifier. Depending on the application, two parameters characterize this power: the input power corresponding to 1 dB of gain compression \( P_{1dB} \) (or output power \( P_{1dB} \)) or the third-order intercept point of input \( I_{P3_E} \) (or output \( I_{P3_A} \)). These quantities will be defined precisely in Chapter 2, which is dedicated to power amplification. In combination with the noise factor, they enable us to define the linear dynamic range of the amplifier.

\[ \text{Dynamic}_{(dB)} = P_{E_{dBm}} - \text{Noise}_{(dBm)} \]

There is another definition for dynamic range, more oriented toward applications in digital communication systems, called SFDR (Spurious Free Dynamic Range), which involves sensitivity and maximum power of the third-order intermodulation spectral components.

The sensitivity defines the minimum input power to ensure an output signal-to-noise ratio (SNR). The value of the signal-to-noise ratio is a function of the bit error rate and the type of modulation.

\[ \text{Sens}_{(dBm)} = \left( \frac{S}{N} \right)_{(dB)} + \text{Noise}_{(dBm)} \]

The input power is limited such that the power of intermodulation spectral components remains below the noise floor.

\[ P_{I_{P3}} \leq \text{Noise}_{(dBm)} \Rightarrow P_{E_{max}}(dBm) = \frac{2I_{P3_E}(dBm) + \text{Noise}_{(dBm)}}{3} \]

\[ \text{SFDR}_{(dB)} = \left( \frac{I_{P3_E}(dBm) - \text{Noise}_{(dBm)}}{3} \right) - \left( \frac{S}{N} \right)_{(dB)} \]
– In addition, DC power consumption, power efficiency, supply voltage and current, stability factor, etc.

1.1.2. Review on active two-port networks in linear mode

Let us consider an active two-port network loaded at port 1 by a generator with internal impedance $Z_1$ (reflection coefficient $\Gamma_1$) and at port 2 by a load with impedance $Z_2$ (reflection coefficient $\Gamma_2$). The two-port network is characterized by its scattering matrix $S$ (Figure 1.4).

![Figure 1.4. Linear active two-port network](image)

Let us recall the main properties of active two-port networks in linear mode. The results are detailed in [GAU 07].

1.1.2.1. Input and output port impedances

The reflection coefficients at both ports are given by the following relations:

$$S'_{11} = \frac{S_{11} - \Delta_3 \Gamma_2}{1 - S_{22} \Gamma_2} \quad S'_{22} = \frac{S_{22} - \Delta_3 \Gamma_1}{1 - S_{11} \Gamma_1}$$  \[1.1\]

1.1.2.2. Transducer power gain

Transducer power gain is the ratio between the power dissipated in the load $P_2$ and the power available at the generator terminals $P_{\text{avail}}$.

$$G_T = \frac{P_2}{P_{\text{avail}}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_1|^2\right) \left(1 - |\Gamma_2|^2\right)}{|(1 - S_{11} \Gamma_1)(1 - S_{11} \Gamma_1) - S_{12} S_{21} \Gamma_1 \Gamma_2|^2}$$  \[1.2\]

1.1.2.3. Stability conditions

The two-port network is unconditionally stable if the impedances at both ports have positive real parts whatever the impedances presented at the same ports.
The two-port network is unconditionally stable if the following two conditions are met simultaneously:

\[
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |A_S|^2}{2|S_{12}S_{21}|} > 1 \quad \text{and} \quad |A_S| < 1
\]  

[1.3]

If not, the two-port network is said to be potentially unstable, which means that there are impedance values to be presented at a port, inducing an impedance at the other port with a negative real part.

The stability circles at ports 1 and 2 in the Smith chart show the zones that cannot be used for reasons of stability.

![Stability circle in the generator plane](image)

**Figure 1.5. Stability circle in the generator plane**

1.1.2.4. Maximum power transfer: maximum gain

The maximum power transfer is obtained when the complex conjugate matching conditions are simultaneously met at both ports.

\[
\Gamma_1 = S_{11}^* \quad \text{and} \quad \Gamma_2 = S_{22}^*
\]

Under these conditions, maximum power transfer is at port 1 between the generator and the two-port network input and at port 2 between the two-port network output and the load. Transducer power gain is then also maximum.
It can be shown that this operation is only possible if the two-port network is unconditionally stable. In this case, there is an optimum couple value to be presented at the two-port network ports for maximum gain.

\[
\Gamma_{m1} = \frac{B_1 - 2|S_{12}S_{21}|\sqrt{K^2 - 1}}{2C_1} \quad \Gamma_{m2} = \frac{B_2 - 2|S_{12}S_{21}|\sqrt{K^2 - 1}}{2C_2}
\]

\[
B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta_s|^2 \quad B_2 = 1 - |S_{11}|^2 + |S_{22}|^2 - |\Delta_s|^2
\]

\[
C_1 = S_{11} - S_{22}^*\Delta_s \quad C_2 = S_{22} - S_{11}^*\Delta_s
\]

The gain is maximum and is equal to: \( G_{r_{\text{max}}} = \left| \frac{S_{21}}{S_{12}} \right| (K - \sqrt{K^2 - 1}) \) \[1.5\]

### 1.1.2.5. Constant gain circles

For some applications, such as low-noise amplifiers, it may be interesting to analyze the influence of the impedance presented at one port when the other is matched.

This leads to the definition of two gains that are two special cases of transducer power gain:

- **Power gain** considering \( \Gamma_1 = S_{11}^* \):

\[
G_p = \left. \frac{P_2}{P_1} \right|_{\Gamma_1 = S_{11}^*} = \frac{P_2}{P_{\text{avai}}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_2|^2\right)}{\left(1 - |S_{11}|^2\right) + \left(|S_{22}|^2 - |\Delta_s|^2\right)|\Gamma_2|^2 - 2\Re(C_2 \Gamma_2)} \] \[1.6\]

- **Available power gain** considering \( \Gamma_2 = S_{22}^* \):

\[
G_d = \left. \frac{P_2}{P_{\text{avai}}} \right|_{\Gamma_2 = S_{22}^*} = \frac{P_{\text{avai}}}{P_{\text{avai}}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_1|^2\right)}{\left(1 - |S_{22}|^2\right) + \left(|S_{11}|^2 - |\Delta_s|^2\right)|\Gamma_1|^2 - 2\Re(C_1 \Gamma_1)} \] \[1.7\]

The set of coefficient values that correspond to a constant value of a given gain is located in a family of circles parameterized by the gain value.

An example of a circle with constant available gain is shown in Figure 1.6.
1.1.2.6. Noise factor

The noise factor characterizes the degradation of the signal-to-noise ratio between the input and output of the device. Since the powers involved are available power levels, the noise depends only on the impedance presented by the generator at port 1. The ratio is evaluated for a generator impedance set at a reference temperature $T_0 = 290$ K.

$$F = \left( \begin{array}{c} S_{1\text{avai}} \\ N_{1\text{avai}} \\ S_{2\text{avai}} \\ N_{2\text{avai}} \end{array} \right) \bigg|_{T = T_0 = 290K}$$

The notion of additional noise temperature is sometimes used. It characterizes the noise power added by the two-port network backed to the two-port network input:

$$\frac{N_{\text{Aavai}}}{G_{\text{Avai}}} = kT_A \Delta f$$

It is linked to the noise factor by:

$$F = 1 + \frac{T}{T_0} \left( \frac{1}{G_{\text{avai}}} - 1 \right)$$
The influence of the impedance at port 1 is defined using three parameters called the noise parameters of the two-port network:

- \( F_{\text{min}} \) Minimum noise factor
- \( Y_{\text{opt}} \) Optimum noise admittance
- \( R_N \) Noise resistance

The two-port network noise factor is expressed in terms of three noise parameters and admittances situated at port 1.

\[
F = F_{\text{min}} + \frac{R_N}{\Re(Y_1)} \left| Y_1 - Y_{\text{opt}} \right|^2
\]  

[1.10]

The noise factor is at its minimum \( F_{\text{min}} \) when the internal admittance, positioned at port 1, is equal to the optimum noise admittance \( Y_{\text{opt}} \). The difference between \( F \) and \( F_{\text{min}} \) for the same value \( Y_1 \) is proportional to noise resistance \( R_N \).

For a reciprocal two-port network, noise is only of thermal origin, so the noise factor depends only on temperature.

\[
F = 1 + \frac{T}{T_0} \left( \frac{1}{G_{\text{avai}}} - 1 \right)
\]  

[1.11]

1.1.2.7. Constant noise factor circles

It is possible to define noise parameters using the concept of an optimum noise reflection coefficient \( \Gamma_{\text{opt}} \) and a normalized noise resistance \( r_N \).

\[
\Gamma_{\text{opt}} = \frac{1 - Z_0 Y_{\text{opt}}}{1 + Z_0 Y_{\text{opt}}} \quad r_N = \frac{R_N}{Z_0}
\]  

[1.12]

Equation [1.10] is then written as:

\[
F = F_{\text{min}} + \frac{4r_N}{\left|1 + \Gamma_{\text{opt}}\right|^2} \left| \Gamma_1 - \Gamma_{\text{opt}} \right|^2
\]  

[1.13]
The set of impedance reflection coefficients at port 1, giving a constant noise factor, is located in a family of circles parameterized by the value of the noise factor. An example of circles of constant noise factor is shown in Figure 1.7.

\[ N = \frac{F - F_{\text{ref}}}{4\pi} + |\Gamma| \]

\[ O_r = \frac{\Gamma_r}{1 + N} \]

\[ R_n = \frac{1}{1 + N} \left( \frac{1}{\Gamma^-} \left[ \frac{N^2 + N(1 - F)}{F} \right] \right) \]

**Figure 1.7. Constant noise factor circles**

1.1.2.8. *Cascade association of two-port networks: Friis formula*

The noise factor of a cascade association of two-port networks is obtained by applying the Friis formula.

\[ F = F_1 + \frac{F_2 - 1}{G_{av1}} + \frac{F_3 - 1}{G_{av1}G_{av2}} + \ldots + \frac{F_n - 1}{G_{av1} \ldots G_{av(n-1)}} \quad [1.14] \]

This relation highlights the importance of the first stage, which must be of low noise and high gain. This remark is particularly pertinent for the design of low-noise amplifiers.

1.1.3. *Basic structure of an amplifier*

The performance of an active two-port network in linear mode, consisting of a transistor and passive components, is based on the following parameters:

- transistor characteristics: technology (heterojunction bipolar transistor (HBT), metal semiconductor field effect transistor (MESFET), pseudomorphic high electron mobility transistor (PHEMT), etc.), sizes (length and width of the gate or base, etc.);
- DC polarization point;
- value of impedances presented at ports 1 and 2.
The choice of these parameters depends on the specifications of the amplifier:
– operating frequency and bandwidth;
– output power;
– gain or noise factor value;
– stability, and so on.

Impedances at amplifier ports are standardized to $Z_0$ (usually 50 $\Omega$). Therefore, it is necessary to include impedance matching two-port networks, both upstream and downstream of the transistor, for which the role is to transform impedance $Z_0$ into an impedance whose value corresponds to $\Gamma_1$ or $\Gamma_2$ (Figure 1.9).

The synthesis of matching two-port networks is essentially a function of amplifier bandwidth and the technology (lumped or distributed elements, with or without losses).

1.1.4. Reciprocal and lossless impedance matching networks

If the matching network is reciprocal and lossless, the amplifier topology has remarkable properties as shown in Figure 1.9.

First, we note that for a reciprocal and lossless two-port network, if the power transfer at one port is maximum, then it is also maximum at the other port.

![Figure 1.9. Basic structure with matching network](image_url)
Figure 1.10. Impedance transformation: reciprocal and lossless two-port network

Two situations may occur in this case:

– The impedances presented at the ports match the maximum power transfer conditions:

\[ \Gamma_1 = S_{11}^* \quad \text{and} \quad \Gamma_2 = S_{22}^* \]

Therefore, \( \Gamma_{E1} = \Gamma_S^* = 0 \) and \( \Gamma_{E2} = \Gamma_L^* = 0 \)

The conditions for maximum power transfer at the transistor ports correspond to the absence of reflected waves at the amplifier ports.

– The presented impedances do not correspond to the conjugate match:

\[ \Gamma_1 \neq S_{11}^* \quad \text{or} \quad \Gamma_2 \neq S_{22}^* \]

In this case, \( \Gamma_{E1} \neq 0 \) or \( \Gamma_{E2} \neq 0 \)

We can then show (Appendix 1):

\[ |\Gamma_{E1}| = \left| \Gamma_1 - S_{11}^* \right| \quad \text{or} \quad |\Gamma_{E2}| = \left| \Gamma_2 - S_{22}^* \right| \]

1.1.5. Design methodology

The design methodology presented here is not unique, but it is very progressive and can be adaptable for most amplifiers.
– Transistor selection and testing:

This step first consists of choosing the transistor according to specifications (type of technology, gain, bandwidth, noise factor, etc.), then determining the static polarization point and, finally, simulating (or measuring) the scattering matrix to calculate the theoretical values of different characteristics and analyze stability.

– Stabilization circuits:

If the transistor is not unconditionally stable in the frequency band of operation, it is necessary to introduce one or more elements into the topology to ensure stability.

– Transistor polarization circuits:

Static polarization of the transistor requires circuitry allowing continuous values to be applied to the transistor without affecting dynamic operation. This can be achieved either using specific circuits or by using slightly modified impedance matching circuits. At this stage, it is essential to study the influence of polarization circuits on the stability of the entire system, especially outside the frequency band of operation (low frequencies).

– Impedance matching circuits:

The choice of the impedance matching circuit is directly related to the operation bandwidth of the amplifier. If several topologies are possible, it may be worthwhile considering the possibility of using these circuits to induce DC polarization.

We will now briefly summarize the main points of this methodology for different types of amplifiers, ranging from narrowband amplifiers with high gain, to low-noise amplifiers and, finally, to wideband amplifiers.

1.2. Narrowband amplifiers with maximum gain

In this section, we will use the characteristics of a PHEMT transistor as an example. It consists of four gate fingers that are 50 µm wide and 0.2 µm long.

1.2.1. Transistor test

First, we select a DC polarization point in the linear region of the transistor to the drain voltage, and to obtain the maximum gain for the grid voltage ($V_{DS} = 3\, \text{V}$ and $V_{GS} = 0\, \text{V}$).

The plot for maximum transducer gain and the stability factor for the polarization point as a function of frequency allow us to determine the frequency
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region wherein the transistor is unconditionally stable. A sample of results is shown in Figure 1.11.

When the stability factor is less than 1, the maximum transfer gain is not defined, and it is replaced by the maximum stable gain plot \( G_{MS} = \left| \frac{S_{21}}{S_{12}} \right| \), obtained with \( K = 1 \).

![Figure 1.11. Maximum gain and stability factor](image)

This result is confirmed by plotting the stability circles at ports 1 and 2 as a function of frequency. This plot also allows us to view the impedance regions for which the transistor is potentially unstable (Figure 1.12).

![Figure 1.12. Stability circles at ports 1 and 2 as a function of frequency](image)
The transistor is unconditionally stable for a frequency above 33.4 GHz. For operation at a higher frequency, the transistor can be used directly.

For operation at a lower frequency, the plot of the stability circles and constant gain circles at ports 1 and 2 confirms that simultaneous power matching at the two ports is not possible (Figure 1.13). It is therefore necessary to stabilize the transistor by adding stabilization circuits.

![Constant gain circles and stability circle](cerclesagainenpuissanceconstantetcercledestabiliteindep(SP3.L_StabCircle1)(0.000to51.000))

**Figure 1.13. Constant gain circles and stability circle**

### 1.2.2. Stabilization circuits

By examining the expression of the stability factor, we see that a decrease in the $|S_{12}S_{21}|$ term increases the value of the stability factor. A simple method to stabilize the transistor is reducing the gain.

The circuit topologies described here use a field-effect transistor; they are readily transferable to bipolar transistors.

#### 1.2.2.1. Resistive stabilization

The decrease in gain is obtained through power dissipation by inserting a resistor into the circuit. Figure 1.14 shows the different topologies possible.

The main advantage of this type of solution is the bandwidth, as power dissipation is almost insensitive to frequency.

The main disadvantages are an increase in power dissipation and additional noise. The latter can be minimized by placing the resistor at the transistor output either in series or in parallel.
The results in Figure 1.15 show that a 10 Ω resistor in series on the grid or a 30 Ω resistor in series on the drain can stabilize the transistor at 20 GHz with the same stability factor (1.3) and maximum gain (10.9 dB) values. On the contrary, they confirm that the degradation of the noise factor is much greater when using a resistor on the grid (0.8 dB instead of 0.2 dB).

1.2.2.2. Reactive stabilization

To eliminate the bad effects related to power dissipation and noise factor, it is possible to use purely reactive feedback impedances in order to bring down the gain (Figure 1.16).
The major disadvantages of this solution are a weak influence on the stability factor and an increased dependence on frequency. The main advantage is that the minimum noise factor of the transistor is not degraded.

![Graph 1](image1.png)

**Figure 1.17. Reactive stabilization**

The results in Figure 1.17 show that an inductor connected in the feedback series to the source stabilizes the transistor at 20 GHz with a stability factor (1.05) and maximum gain (10.7 dB); the minimum noise factor remaining virtually unchanged.

This analysis can be completed by plotting constant gain circles to the operating frequency, parameterized by the feedback impedance value.

These plots confirm the need for a compromise between improving the stability factor and reducing the maximum gain. They also show a decrease in reflection coefficient modules corresponding to the maximum power transfer, thus facilitating the design of impedance matching networks.

Figure 1.18 shows these plots for two values: the first corresponding to the stability limit and the second corresponding to an acceptable compromise.

![Graph 2](image2.png)

**Figure 1.18. Stabilization: constant gain availability circles**
1.2.3. Polarization circuits

These circuits must allow DC polarization to be brought onto the transistor without affecting the dynamic operation of the amplifier. The circuits shown correspond to a field-effect transistor and can be easily transposed onto the bipolar transistor.

Only the part directly interacting with dynamic microwave operation is analyzed. Conventional electronic circuitry for the generation of continuous voltage or current is not considered.

1.2.3.1. Use of specific circuits

Three elements are necessary for polarization:

– The first element ensures electrical continuity between the voltage supply and the transistor electrode (grid or drain). Under dynamic conditions, this element is located between the electrode and the mass; therefore, the impedance presented to the operating frequency must be very high.

– The second element is used to isolate the remainder of the DC voltage circuit so that the latter is not present at the amplifier ports. In a dynamic system, this element is located in series with the electrode; therefore, the impedance presented to the operating frequency must be very low.

– The third element is used to decouple the DC supplies so that, under dynamic conditions, the internal impedance of the power supply is close to short-circuit.

Figure 1.19 shows some circuit topologies using lumped elements such as resistors, capacitors and inductors.

– Circuit A is the most classical. The elements ensuring DC isolation are the \( C_L \) capacitors (called bond) whose values must be large enough such that their impedances are very low (for example, impedance lower than 1\( \Omega \) at 20 GHz is obtained with a capacitor above \( 8pF \)). The electrical continuity is ensured by the \( L_C \) inductors (called polarization or shock) whose values must be large enough such that their impedances are very high (for example, impedance higher than 1,000\( \Omega \) at 20 GHz is obtained with an inductor above \( 8nH \)). Decoupling of power is achieved with \( C_D \) capacitors (the so-called decoupling) for which the value must be sufficiently high. In practice, the value of impedance in the operating band should be lower than that of the bond capacitor.

Polarization inductors can be replaced by sufficient value resistors in order not to disturb the dynamic operation; then there exists a DC voltage across resistors, which causes an increase in power dissipation. This technique is difficult to use on
the drain when the current is greater than a few mA, but it is quite applicable on the grid for which direct current is negligible.

– Circuit B uses the self-polarization technique, which only uses one DC power supply. Grid polarization is obtained by making the grid potential equal to zero by means of a high value resistor $R_G$ and making the source potential a positive value due to a voltage drop across the resistors in series on the grid $R_S$. This resistor is decoupled in dynamic mode with a capacitor $C_S$ for which the value is chosen so as not to degrade the gain too much. This resistor can also be used to stabilize the transistor (see section 1.2.2).

– Circuit C uses an active load, which is a transistor polarized to $V_{GS} = 0$. In dynamic state, the impedance presented corresponds to the first order of the inverse of the output conductance of the transistor; so at a relatively high value, this will moderately affect the gain. In steady state, it is easy to see from Figure 1.19 that this resistor is much lower and therefore limits the DC voltage drop. This solution is mainly used in monolithic integrated circuits.

![Diagram of polarization methods](image)

**Figure 1.19. DC polarization: lumped specific circuits**

Figure 1.20 shows a topology that uses distributed circuits such as transmission lines. It uses properties of the quarter-wave line terminated by a short or an open circuit. The operation is inherently narrowband around the frequency for which the lines are quarter-wave lines. It is possible to expand this band by correctly choosing the characteristic impedances of the lines (see Figure 1.20).
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![Diagram](image)

Properties of the quarter-wave line

\[
Z_0 = \frac{Z_0^2}{Z}
\]

\[Z_0 = 0 \Rightarrow Z_0 = \infty \]

\[Z_\infty = 0 \Rightarrow Z_\infty = 0\]

**Figure 1.20. DC polarization: distributed specific circuits**

1.2.3.2. Use of impedance matching circuits

The use of matching circuits to ensure polarization reduces the number of elements to be added to the circuit. The operation is through a wider band; it operates at least in the matching circuit’s bandwidth.

Not all matching circuits are suitable for this; it is necessary for the matching circuit topology to provide electrical continuity between the mass and the transistor electrode.

Figure 1.21 shows an example of lumped impedance matching and the necessary modifications to enable polarization of the component. In particular, we see that it suffices to connect the parallel element to the mass via a decoupling capacitor \( C_D \) for which the value is sufficiently high.

![Diagram](image)

**Figure 1.21. DC polarization: impedance matching circuits**
Figure 1.22 shows an example using distributed elements for which the input circuit does not provide electrical continuity and therefore does not allow polarization of the transistor. It is therefore necessary to use a specific polarization circuit at input. However, the output circuit can easily lead to polarization.

**Figure 1.22.** DC polarization: impedance matching circuits

### 1.2.4. Polarization circuits and stability

By reviewing the performance of stabilization circuits, we found that stabilization is effective in the operating band and beyond; but in most cases, the transistor is potentially unstable below a certain frequency. Therefore, impedance values exist at low frequencies which are likely to oscillate the amplifier. They are located in the Smith chart in areas around the unit circle and sometimes adjacent to the short or open circuit (Figure 1.12).

Furthermore, the impedances presented by polarization circuits are also located in the short-circuit neighborhood. Figure 1.23 gives an example of impedance presented on the transistor drain by a polarization circuit using a quarter-wave line between 1 and 10 GHz for an operating frequency of 20 GHz. By overlapping the stability circles at transistor outputs in the same frequency band, we find that the impedances are located in areas of potential instability.

It is therefore necessary to stabilize the transistor outside the operating band, especially at low frequencies.
The most frequently used method is to introduce further power dissipation outside the operating band by inserting a resistor either in the polarization circuit, or in series with the grid or drain of the transistor. The effect of this resistance is adjusted in relation to the frequency using a decoupling capacitor for which the value is adjusted to obtain a good gain-stability compromise.

Figure 1.24 shows two examples: the first example uses a resistor in the polarization circuit and the second example introduces a resistor in series in the matching circuit.

![Figure 1.23. Stability and polarization](image)

![Figure 1.24. Out of operating band stabilization](image)
Figure 1.25 shows the influence of the adjustment of the capacitor $C_p$ on the stability factor when the resistor is placed in the polarization circuit.

![Graph showing the influence of $C_p$ on stability factor](image)

**Figure 1.25. Out-of-band stabilization: compromise adjustment**

### 1.2.5. Impedance matching circuits

The topology of matching circuits is a function of the value of the amplifier operating frequency bandwidth. The topologies presented in this section correspond to narrowband amplifiers with bandwidths not exceeding a few tens of %. In this case, the circuit will only be considered at the central frequency of operation $f_0$.

As the objective is to obtain maximum gain, the matching circuits are chosen to be reciprocal and lossless, and the matching in wave meaning will therefore be satisfied automatically at the amplifier ports. To minimize parasitic and coupling elements, topologies are usually as simple as possible.

The components of the circuits can either be lumped (inductor, capacitor) or distributed constants (transmission line segments). The type of the element depends on the frequency band and technology. Lumped circuits are used in the lower part of the microwave band. Since circuits with distributed constants are reserved for the higher part of the same frequency band, the limit is heavily related to the technology used (monolithic integrated circuits or hybrid circuits).

#### 1.2.5.1. Single-stage amplifier: input and output matching

Figure 1.26 recalls the impedance matching conditions to obtain the maximum transducer power gain. These conditions are only possible for an unconditionally stable transistor, which means that the parameters to be used are those of the transistor associated with stabilization and polarization circuits.
Figure 1.26. Matching conditions for maximum gain

The matching conditions for maximum gain are:

\[
\begin{align*}
\Gamma_1 &= S_{11}^* \\
\Gamma_2 &= S_{22}^* \\
\Rightarrow \quad \Gamma_1 &= \Gamma_{m1} \\
\Gamma_2 &= \Gamma_{m2}
\end{align*}
\]

[1.16]

A matching circuit must allow conversion of the reference impedance \( Z_0 \) to an impedance that contains a determined real part and an imaginary part. Such a circuit must have at least two degrees of freedom.

1.2.5.2. Lumped circuits

Figure 1.27 shows the lumped topologies that are widely used. The circuits comprise pure reactive impedances. There is an area of unmatchable impedances for each topology.

Figure 1.27. Topologies of lumped matching circuits
The equations allow us to easily determine $b_1$ and $b_2$ (respectively, $x_1$ and $x_2$) if we know $\Re(y_1)$ and $\Im(y_1)$ (respectively, $\Re(z_1)$ and $\Im(z_1)$). The choice of topology depends on the value of $\Re(y_1)$ (respectively, $\Re(z_1)$).

Topology 1: $y_1 = Z_0 Y_1$ $\quad$ tq $\Re(y_1) < 1$ $\quad\Rightarrow b_2 = \pm \sqrt{\frac{\Re(y_1)}{1 - \Re(y_1)}}$

- $b_2 > 0 \Rightarrow b_2 = Z_0 C_x \omega$
- $b_2 < 0 \Rightarrow b_2 = -\frac{Z_0}{L_x \omega}$

$\Rightarrow b_1 = \Im(y_1) - \frac{b_2}{1 + b_2^2}$ $\Rightarrow \quad \{ b_1 > 0 \Rightarrow b_1 = Z_0 C_x \omega \}$
$\quad$ $\{ b_1 < 0 \Rightarrow b_1 = -\frac{Z_0}{L_x \omega} \}$ \quad [1.17]

Topology 2: $z_1 = \frac{Z_1}{Z_0}$ $\quad$ tq $\Re(z_1) < 1$ $\quad\Rightarrow x_2 = \pm \sqrt{\frac{\Re(z_1)}{1 - \Re(z_1)}}$

- $x_2 > 0 \Rightarrow x_2 = \frac{L_x \omega}{Z_0}$
- $x_2 < 0 \Rightarrow x_2 = -\frac{1}{Z_0 C_x \omega}$

$\Rightarrow x_1 = \Im(z_1) - \frac{x_2}{1 + x_2^2}$ $\Rightarrow \quad \{ x_1 > 0 \Rightarrow x_1 = \frac{L_x \omega}{Z_0} \}$
$\quad$ $\{ x_1 < 0 \Rightarrow x_1 = -\frac{1}{Z_0 C_x \omega} \}$ \quad [1.18]

There are at least two solutions for the same impedance to be matched. The choice must involve other factors such as the ease of technological achievement and the possibility of using the circuit to polarize the transistor. Figure 1.28 shows two examples of matching circuits.

![Figure 1.28. Examples of lumped matching circuits](image-url)
1.2.5.3. *Distributed circuits*

Circuits consist of transmission line segments; the design parameters include the length of the line and the value of characteristic impedances.

Figure 1.29 shows some examples of circuits with distributed constants.

![Figure 1.29. Examples of matching circuits with distributed constants](image)

The values of the elements in these circuits are obtained either analytically or graphically using the Smith chart.

As an example, let us consider a single stub circuit.

The analytical calculation of normalized input admittance relative to $Z_0$ gives:

$$y_1 = \frac{1 + j(\theta_1 + \theta_2)}{1 - \tan \theta_2 + j \tan \theta_1}$$

with $\theta_1 = \frac{2\pi d_1}{\lambda}$, $\theta_2 = \frac{2\pi d_2}{\lambda}$, $Z_{01} = Z_{02} = Z_0$

Then we have to equalize the real and imaginary parts to those of the desired admittance.

The graphical method is illustrated in Figure 1.30.

As for lumped circuits, the choice of topology is related to the difficulties of technological achievement (for example, grounding by via hole) or to the possibility of using the circuit to polarize the transistor (electrical continuity).
1.2.5.4. Lumped-distributed mixed circuits

In some cases, it can be interesting to combine the two types of elements. This is called a lumped-distributed mixed circuit.

Figure 1.31 shows some examples of this.

1.2.6. The multistage amplifier: inter-stage matching

When the gain obtained through a single transistor is insufficient, it is necessary to cascade two or more elementary amplifiers as shown in Figure 1.32.
The available power gain of the amplifier is equal to the product of the available power gains of each amplifier. When the amplifiers are matched, the available power gains become equal to the transducer gains.

When amplifiers are not matched, the use of flow graphs allows us to take the phenomena of multiple reflections due to mismatches into account. This approach is costly in terms of components as it requires passing through the reference impedance $Z_0 = 50\,\Omega$ at each interconnection. It is justified for analyzing the assembly of subsets.

As part of the design for an amplifier subset, it is preferable to remove this passage through $Z_0$ by concatenating the output and input matching circuits at interconnected ports to a single circuit called an interstage matching circuit (Figure 1.33).

**Figure 1.33. Interstage matching**

Impedance matching conditions for interstage circuit then become:

\[
\Gamma_2' = S_{22}^{**} = \Gamma_{m2T1} \\
\Gamma_1'^* = S_{11}^{**'} = \Gamma_{m1T2}
\]  

[1.19]

### 1.2.7. Design example

To illustrate the above results, we show the simulation results of an amplifier operating at a frequency of 20 GHz.
The transistor is stabilized by a reactive feedback in the source, using a short-circuited transmission line section.

Maximum gain matching is possible with optimum impedances $\Gamma_{m1}$ and $\Gamma_{m2}$ (equation [1.4]). We obtain out-of-band stabilization using a resistor in the polarization circuit and a decoupling capacitor for which the value has been optimized.

Figure 1.34 shows the results that are consistent with theoretical predictions:
– unconditionally stable amplifier, whatever the frequency ($K > 1$);
– input and output matching ($< -50$ dB);
– maximum gain at the central frequency (10.4 dB).

The frequency bandwidth for a reflection coefficient less than $-15$ dB is approximately 5%.

![Figure 1.34. Example of narrowband amplifier with maximum gain](image)

1.3. Low-noise narrowband amplifier

1.3.1. Review of the noise characteristics of a transistor

The noise parameters of a transistor have been defined in section 1.1.2.6; there exists an optimum value of impedance which must be presented at the transistor
input to obtain the minimum noise factor. Variation of the noise factor depending on impedance is given by equation [1.10] and can be seen in the constant noise factor circles in Figure 1.7. Among the criteria for the selection of a transistor, there is of course a minimum noise factor $F_{\text{min}}$, but we must also consider the resistor noise value $R_N$, which should be low.

An additional feature is the associated gain that is set when the transistor is loaded by impedances, ensuring the minimum input noise factor and maximum output power transfer (Figure 1.35).

$$G_{\text{ass}} = \frac{|S_{21}|^2 (1 - |\Gamma_{\text{opt}}|^2)}{|1 - S_{11} \Gamma_{\text{opt}}|^2 - S_{22} - \Delta_S \Gamma_{\text{opt}}|^2}$$

**Figure 1.35.** Definition of associated gain from a two-port network

The minimum noise factor depends on the DC polarization of the transistor. There is a polarization that allows us to minimize the minimum noise factor. Figure 1.36 shows the variation in minimum noise factor and associated gain as a function of grid polarization voltage for a HEMT-type transistor. As these two parameters are not optimum for the same polarization value, it is necessary to find a compromise in order to maintain an acceptable gain without excessively degrading the noise factor.

**Figure 1.36.** Minimum noise factor and DC polarization
The minimum noise factor increases with frequency in a virtually linear manner; it also increases with the unit length of grid fingers and decreases with the number of fingers at constant total development. For example, for the transistor used previously at 20 GHz, $F_{\text{min}}$ is 1.55 dB for four 50 µm fingers and 1.3 dB for eight 25 µm fingers.

1.3.2. Minimum noise factor amplifier

The design methodology is identical to that of a maximum gain amplifier. After choosing the transistor type and the polarization point (section 1.3.1), it must be polarized and eventually stabilized.

In order not to deteriorate the noise factor, stabilization by reactance in the source will be used (Figure 1.16). Similarly, the out-of-band stabilization will be preferentially achieved by a resistor in the polarization circuit (Figure 1.24).

The impedance matching circuits may be the same type as those described above. Nonetheless, it is important to consider the input losses from the matching circuit as a criterion for choice so that the noise factor is not deteriorated.

Indeed, if we denote the available power gain of the input matching circuit by $G_{d1}$ and the noise factor of the transistor by $F_2$, the application of the Friis formula gives:

\[
F_{I} = \frac{1}{G_{d1}} \quad \text{if } T = T_0
\]

\[
F_T = F_I + \frac{F_2 - 1}{G_{d1}} = \frac{F_2}{G_{d1}} Q_{\text{1passive}} \Rightarrow G_{d1} < 1 \Rightarrow F_T > F_2
\]

\[
A_{d1(dB)} = -G_{d1(dB)} \Rightarrow F_{T(dB)} = F_2(dB) + A_{d1(dB)}
\]

[1.20]

Degradation of the amplifier noise factor is directly affected by losses from the input matching network. Therefore, it is necessary to minimize losses from the input matching circuit.

Impedances to be presented at the transistor ports are different from those corresponding to maximum gain. The minimum noise factor fixes the value of impedance at the input; the output impedance is then chosen to ensure maximum power transfer to this port.

\[
\begin{align*}
\Gamma_1 &= \Gamma_{\text{opt}} \\
\Gamma_2 &= S_{22}^{*} \quad \Gamma_1 = \Gamma_{\text{opt}}
\end{align*}
\]

[1.21]
The obtained gain is then the transistor-associated gain.

\[
G_{axx} = \frac{|S_{21}|^2 \left(1 - |\Gamma_{opt}|^2 \right)}{|1 - S_{11} \Gamma_{opt}|^2 - |S_{22} - \Delta_S \Gamma_{opt}|^2}
\]  

[1.22]

As the maximum power transfer is not verified upon input, the reflection coefficient at the amplifier input is non-zero. It can be expressed using equation [1.15].

\[
|\Gamma_{E1}| = \left| \frac{\Gamma_{opt} - S_{11}^*}{1 - S_{11} \Gamma_{opt}} \right| \text{ with } S_{11} = \frac{C_1 - (|S_{11}|^2 - |\Delta_S|^2)\Gamma_{opt}^*}{1 - |S_{22}|^2 - C_1 \Gamma_{opt}^*} \text{ and } C_1 = S_{11} - S_{22}^* \Delta_S
\]  

[1.23]

The maximum transfer of output power allows the amplifier output matching to be obtained: \( |\Gamma_{E2}| = 0 \).

Figure 1.37 shows the simulation results for an amplifier identical to that given in section 1.2.7, except for the impedance matching circuits.

**Figure 1.37. Example of a narrowband amplifier with minimum noise factor**

The results are consistent with theoretical results:
- noise factor equal to the minimum noise factor (1.7 dB);
- lower gain than maximum gain (9.05 dB instead of 10.4 dB);
- output matching (\(<-50\) dB) and mismatch at the input (\(<-7.6\) dB).
1.3.3. Noise factor–gain matching compromise

Input mismatch is directly related to the difference between minimum noise factor and maximum power transfer conditions.

This difference can be reduced by applying reactive feedbacks to the transistor.

The most commonly used technique is to place an inductive feedback in the source, which is simple to implement and also serves to stabilize the transistor.

The plots of constant available gain and constant noise factor circles for several values of the feedback impedance presented in Figure 1.38 allow us to draw the following conclusions, when increasing the influence of feedback:

– Noise circles barely change.

– The conditions for maximum power transfer get closer to those corresponding to minimum noise factor.

– The maximum gain decreases.

– The gap between associated gain corresponding to minimum noise factor and maximum gain decreases.

![Figure 1.38. Gain–noise factor compromise](image-url)
The reflection coefficient at the input of the amplifier can be expressed in terms of the gap between available gain and maximum gain:

\[ |\Gamma_{E1}|^2 = 1 - \frac{G_{d(G_1)}}{G_{d_{\text{max}}}} \]  \[1.24\]

Equation [1.24] simply indicates that power that is not transmitted to the output is completely reflected at the input due to the absence of losses in the matching circuits.

If we consider Figure 1.38, the constant gain circle that passes through the point corresponding to the minimum noise factor corresponds to a gain of 9.3 dB and a drop of 1.6 dB in gain, which imposes a reflection coefficient of –5.1 dB. The amplifier is highly mismatched.

We can improve matching by increasing the influence of feedback, which results in assimilating the conditions of maximum noise and maximum gain, as shown by case C in Figure 1.38. In this case, the constant gain circle corresponds to a gain of 8.9 dB and a drop of 0.8 dB in gain, which imposes an input reflection coefficient of –7.7 dB, thus showing that the matching input is improved at the expense of amplifier gain.

Improvement of the reflection coefficient at input without excessive deterioration of gain leads to a necessary acceptance of noise factor degradation.

The search for a compromise can be facilitated by the plot of available gain and constant noise factor circles.

For example, we can use case B of Figure 1.38, repeated in Figure 1.39. Let us suppose that the maximum value of the reflection coefficient is –10 dB, we can deduce the maximum possible drop in gain:

\[ \frac{G_{d(G_1)}}{G_{d_{\text{max}}}} = 1 - |\Gamma_{E1}|^2 \Rightarrow \frac{G_{d(G_1)}}{G_{d_{\text{max}}}} = -.45 \text{ dB} \]

We then only need to search for the point that induces the smallest noise factor in the constant available gain circle, corresponding to a difference of –0.45 dB. This corresponds to searching for the constant noise factor circle tangent to the selected constant available gain circle. In the present case, this circle represents a noise factor degraded by 0.2 dB compared to the minimum noise factor (Figure 1.39).
The end result of this search for a compromise is therefore:

\[ |\Gamma_{E_1}| = -10 \text{ dB} \]
\[ G_d = 9.7 \text{ dB} \]
\[ F = 1.9 \text{ dB} \]

The opposite approach is also possible; it suffices to determine the noise factor and seek the constant available gain circle that is tangent to the retained noise factor circle. We then deduce the reflection coefficient at the input of the amplifier.

### 1.3.4. Multistage amplifier and noise factor

The increase in amplifier gain is limited by the considerations set out in section 1.3.3; therefore, higher gains can only be achieved through the use of multistage structures.

The problem of compromise between noise factor, gain and matching is critical for the first level of the amplifier.

The Friis formula (equation [1.14]) shows that the noise factor of an amplification chain is essentially determined by that of the first stage, provided that the gain is high enough.

The main difficulty arises from the fact that, for a given component, a decrease in the noise factor is accompanied by a decrease in the available gain and, therefore, an increase in the input reflection coefficient. The method for obtaining a compromise as presented in section 1.3.3 here takes on its full importance.
As an example, we consider a two-stage amplifier. The first stage is optimized for noise level and the second is optimized for maximum gain. Let us analyze the influence of the performance of the first stage on the performance of the complete amplifier.

Characteristics of the second stage:

\[
\begin{align*}
G_d & = G_{\text{max}} = 10.9 \text{ dB} \\
F & = 3.7 \text{ dB}
\end{align*}
\]

For the first stage, we consider three cases:

- Case 1: minimum noise factor
  \[
  \begin{align*}
  G_d & = G_{\text{n1}} = G_{d_{\text{max}}}-1.2 = 8.9 \text{ dB} \\
  F & = F_{\text{min}} = 1.76 \text{ dB} \\
  |\Gamma_{E1}| & = -6.1 \text{ dB}
  \end{align*}
  \]

- Case 2: noise factor increased by 0.1 dB
  \[
  \begin{align*}
  G_d & = G_{d_{\text{max}}}-0.6 = 9.5 \text{ dB} \\
  F & = F_{\text{min}} + 0.1 = 1.86 \text{ dB} \\
  |\Gamma_{E1}| & = -8.9 \text{ dB}
  \end{align*}
  \]

- Case 3: noise factor increased by 0.2 dB
  \[
  \begin{align*}
  G_d & = G_{d_{\text{max}}}-0.4 = 9.7 \text{ dB} \\
  F & = F_{\text{min}} + 0.2 = 1.96 \text{ dB} \\
  |\Gamma_{E1}| & = -10.5 \text{ dB}
  \end{align*}
  \]

The performances of each amplifier are determined by applying the Friis formula:

- Case 1:
  \[
  \begin{align*}
  G_d & = 19.8 \text{ dB} \\
  F & = 2.23 \text{ dB} \\
  |\Gamma_{E1}| & = -6.1 \text{ dB}
  \end{align*}
  \]

- Case 2:
  \[
  \begin{align*}
  G_d & = 20.4 \text{ dB} \\
  F & = 2.25 \text{ dB} \\
  |\Gamma_{E1}| & = -8.9 \text{ dB}
  \end{align*}
  \]

- Case 3:
  \[
  \begin{align*}
  G_d & = 20.6 \text{ dB} \\
  F & = 2.33 \text{ dB} \\
  |\Gamma_{E1}| & = -10.5 \text{ dB}
  \end{align*}
  \]

The solution in case 3 seems to be a good compromise with the best matching and therefore the best gain, while only degrading the noise factor by 0.1 dB, in comparison to the solution in case 1, which brings up a very strong mismatch.

1.3.5. Balanced low-noise amplifier

Some transistors have a very large difference between \( \Gamma_{n1} \) and \( \Gamma_{opt} \). In this case, the search for an acceptable compromise can be difficult or impossible.
One solution is to use a balanced amplifier topology using 3 dB/90° directional couplers and two identical amplifiers (Figure 1.40). The amplifiers are designed to obtain the minimum noise factor.

The distribution matrix of an ideal coupler is written as follows:

\[
S = \frac{1}{\sqrt{2}} \begin{pmatrix}
0 & 0 & 1 & j \\
0 & 0 & j & 1 \\
1 & j & 0 & 0 \\
j & 1 & 0 & 0
\end{pmatrix}
\]

The operation of directional couplers is detailed in [PAS 05].

The performance analysis of this circuit can be done using the flow graphs method. This is detailed in [GAU 07]. Figure 1.41 shows the flow graph of the balanced amplifier, including amplifier noise sources and matched loads placed at unused ports.

The scatter matrix and the noise power wave vector of the equivalent two-port network between ports 1 and 2 are as follows (see Appendix 2):

\[
S_{\text{ampli}} = \frac{1}{2} \begin{pmatrix}
S_{B11} - S_{A11} & j(S_{A12} + S_{B12}) \\
j(S_{A21} + S_{B21}) & S_{A22} - S_{B22}
\end{pmatrix}
\]

\[
b_{\text{Nampi}} = \frac{1}{\sqrt{2}} \begin{pmatrix}
jb_{\text{AN1}} + b_{\text{BN1}} + j(S_{A11} + S_{B11})b_{\text{LN3}} + \frac{(S_{B12} - S_{A12})}{\sqrt{2}}b_{\text{LN4}} \\
b_{\text{AN2}} + jb_{\text{BN2}} + \frac{(S_{A21} - S_{B21})}{\sqrt{2}}b_{\text{LN3}} + j(S_{A22} + S_{B22})b_{\text{LN4}}
\end{pmatrix}
\]

\[1.25\]
If both amplifiers are identical, the scattering matrices and correlation matrices are equal: \( S_A = S_B = S \) and \( C_{SA} = C_{SB} = C_S \).

The equations are simplified as:

\[
S_{\text{ampli}} = \begin{pmatrix}
0 & jS_{12} \\
0 & jS_{21}
\end{pmatrix}
\]

\[
C_{\text{ampli}} = \begin{pmatrix}
\langle b_{N1}^* b_{N1} \rangle + |S_{11}|^2 kT \Delta f & 0 \\
0 & \langle b_{N2}^* b_{N2} \rangle + |S_{22}|^2 kT \Delta f
\end{pmatrix}
\]

\[1.26\]

**Figure 1.41. Flow graph of a balanced amplifier**

The noise factor can be expressed in terms of noise power waves; the general expression is simplified when the input closing conditions correspond to matching.

\[
F_{\text{ampli}} = 1 + \frac{\langle b_{N1}^* b_{N1} \rangle}{|S_{21}|^2 kT_0 \Delta f}
\]

Or, after calculation:

\[
F_{\text{ampli}} = F + \frac{|S_{22}|^2 T}{|S_{21}|^2 T_0}
\]

\[1.27\]

In practice, the output of basic amplifiers is matched, wherefrom: \( F_{\text{ampli}} = F \)
The equivalent amplifier between ports 1 and 2 therefore has the following properties:

- Input and output matching regardless of amplifier reflection coefficients, provided that they are equal: it should be noted that the power transfer is not improved: the power reflected at the basic amplifier ports is simply directed toward ports 3 and 4 where it is dissipated in the matched loads.

- Power gain equal to that of a basic amplifier: the output power of each individual amplifier is divided to improve the linearity of the device.

- Noise factor equal to that of the basic amplifier if the latter is matched at output, otherwise the value is slightly higher due to the noise generated by the matched load placed at port 4.

Noise performances are also deteriorated due to coupler losses. In Appendix 2, we show that if the input coupler losses are introduced as $S_{31} = \frac{\alpha}{\sqrt{2}}$ and $S_{41} = j\frac{\alpha}{\sqrt{2}}$, the noise factor of the amplifier is written as:

$$F_{\text{ampli}} = \frac{1}{\alpha^2} \left( F + \frac{|S_{22}|^2}{|S_{21}|^2} \right) + \frac{1-\alpha^2}{\alpha^2 |S_{21}|^2} \tag{1.28}$$

Losses from the input coupler directly degrade the noise factor of the amplifier. This result is comparable to that obtained by the Friis formula for two-port networks.

It may be noted that, in equation [1.25], a mismatch between the amplifiers degrades its operation. However, the system continues to operate and provides a certain operation security for this amplifier.

Finally, an imbalance in the module and/or phase between coupler channels degrades the performance of the balanced amplifier.

1.4. Specific configurations for transistors

In the previous sections, we assumed that transistors were used in common-source configuration (common-emitter) directly connected to the ground or through a feedback in series. In this section, we recall the characteristics of other common-grid (common-base) and common-drain (common-collector) conventional configurations, and also present the performances of the component that are equivalent to a two-transistor cascade: the first with two transistors in common-source configuration and the second with the first in common-source configuration cascaded with a common-grid configuration known as “cascode”.
The reference parameters are those of the common-source configuration. We use the admittance parameters and Pi equivalent circuits, which are simplified to identify the main properties of studied configurations. The results are presented for field-effect transistors and are transferable to bipolar transistors too. Details of the calculation are presented in Appendix 3.

### 1.4.1. Common-grid and common-drain configurations

#### 1.4.1.1. Common-source configuration

The admittance parameters that include noise values for common-source configuration are:

\[
(Y_S) = \begin{bmatrix} Y_{s11} & Y_{s12} \\ Y_{s21} & Y_{s22} \end{bmatrix}, \quad (I_{SN}) = \begin{bmatrix} I_{NG} \\ I_{ND} \end{bmatrix}.
\]  

\[
(C_{YS}) = <(I_{SN})(I_{SN})^+> = \begin{bmatrix} C_{YS11} & C_{YS12} \\ C_{YS21} & C_{YS22} \end{bmatrix} = \begin{bmatrix} <I_{NG}^*I_{NG}> & <I_{NG}^*I_{ND}> \\ <I_{ND}^*I_{NG}> & <I_{ND}^*I_{ND}> \end{bmatrix}.
\]

By using a Pi equivalent circuit as shown in Figure 1.42, we obtain:

\[
(Y_S) = \begin{bmatrix} Y_{s1} + Y_{s3} & -Y_{s3} \\ Y_{sT} - Y_{s3} & Y_{s2} + Y_{s3} \end{bmatrix}
\]  

\[\text{Figure 1.42. Pi equivalent circuit: common-source configuration}\]

For a field-effect transistor, we can use a simplified equivalent circuit, which is valid for frequencies not too high relative to the transition frequency, as represented in Figure 1.43.

\[\text{Figure 1.43. Simplified equivalent circuit: common-source configuration}\]
The elements of the Pi circuit from Figure 1.41 are therefore expressed as follows:

\[
\begin{align*}
Y_{s1} &= \frac{jC_{gs} \omega}{1 + jR_{gs} C_{gs} \omega} = R_{gs} \frac{C_{gs}^2 \omega^2}{1 + j\omega \tau_0} + jC_{gs} \omega \\
Y_{s2} &= g_d + jC_{gs} \omega \\
Y_{s3} &= jC_{gs} \omega \\
Y_{st} &= \frac{g_m e^{-j\omega \tau_0}}{1 + jR_{gs} C_{gs} \omega} = g_m - jg_m \tau_0
\end{align*}
\]

[1.31]

The equations are valid if

\[
\begin{align*}
1 + (R_{gs} C_{gs} \omega)^2 &= 1 \\
e^{-j\omega \tau_0} &= 1 - j\omega \tau_0 \text{ with } \tau = \tau_0 + R_{gs} C_{gs}
\end{align*}
\]

1.4.1.2. Common-grid configuration

The admittance parameters including common-grid configuration noise values are expressed in terms of common-source configuration parameters as:

\[
(Y_G) = \begin{pmatrix}
Y_{s1} + Y_{s12} + Y_{s21} + Y_{s22} & -(Y_{s12} + Y_{s22}) \\
-(Y_{s21} + Y_{s22}) & Y_{s22}
\end{pmatrix}
\]

\[
(I_{GN}) = \begin{pmatrix}
-I_{NG} - I_{ND} \\
I_{ND}
\end{pmatrix}
\]

\[
(C_{YG}) = \begin{pmatrix}
C_{s11} + C_{s12} + C_{s21} + C_{s22} & -C_{s12} - C_{s21} \\
-C_{s12} - C_{s21} & C_{s22} - C_{s12}
\end{pmatrix}
\]

Figure 1.44 shows the common-grid transistor configuration by the Pi equivalent circuit

\[
(Y_G) = \begin{pmatrix}
Y_{st} + Y_{s1} + Y_{s2} & -Y_{s2} \\
-(Y_{st} + Y_{s2}) & Y_{s2} + Y_{s3}
\end{pmatrix}
\]

[1.33]

\[
\begin{align*}
Y_{G1} &= Y_{s1} + Y_{st} \\
Y_{G2} &= Y_{s3} \\
Y_{G3} &= Y_{s2} \\
Y_{GT} &= -Y_{st}
\end{align*}
\]

[1.34]
The elements of this equivalent circuit are expressed as:

\[
\begin{align*}
Y_{G1} &= \left( g_{m0} + R_{gs} C_{gs} \omega^2 \right) + j \left( C_{gs} - g_{m0} \tau \right) \omega \\
Y_{G2} &= j C_{gs} \omega \\
Y_{G3} &= g_d + j C_{ds} \omega \\
Y_{GT} &= -g_{m0} + j g_{m0} \tau \omega
\end{align*}
\]

[1.35]

Note that the output impedance is very high (low \( C_{gd} \)) and the real part of the input admittance is close to \( g_{m0} \); so it is adjustable by choosing the grid width of the transistor (grid development).

1.4.1.3. Common-drain configuration

The admittance parameters including common-drain configuration noise values are expressed in terms of common-source configuration parameters:

\[
\begin{align*}
(Y_D) &= \begin{bmatrix}
Y_{S11} & - (Y_{S12} + Y_{S11}) \\
-(Y_{S21} + Y_{S11}) & Y_{S11} + Y_{S12} + Y_{S21} + Y_{S22}
\end{bmatrix} \\
(I_{DN}) &= \begin{bmatrix}
I_{NG} \\
- I_{NG} - I_{ND}
\end{bmatrix}
\end{align*}
\]

[1.36]

\[
(C_{YD}) = \begin{bmatrix}
C_{YS11} & -C_{YS11} \text{ and } C_{YS12} \\
-C_{YS11} - C_{YS12} & C_{YS11} + C_{YS12} + C_{YS12} \text{ and } C_{YS22}
\end{bmatrix}
\]

We can represent the common-drain transistor configuration by the Pi equivalent circuit as shown in Figure 1.45.

\[
(Y_D) = \begin{bmatrix}
Y_{S1} + Y_{S3} & -Y_{S1} \\
-(Y_{ST} + Y_{S1}) & Y_{ST} + Y_{S1} + Y_{S2}
\end{bmatrix}
\]

[1.37]

Figure 1.45. Pi equivalent circuit: common-drain configuration

\[
\begin{align*}
Y_{D1} &= Y_{S3} & Y_{D2} &= Y_{ST} + Y_{S2} \\
Y_{D3} &= Y_{S1} & Y_{DF} &= -Y_{ST}
\end{align*}
\]

[1.38]
The elements of this equivalent circuit are expressed as:

\[
\begin{align*}
Y_{D1} &= jC_{gd} \omega \\
Y_{D2} &= (g_{m0} + g_d) + j(C_{ds} - g_{m0})\omega \\
Y_{D3} &= R_g C_{gs}^2 \omega^2 + jC_{gs} \omega \\
Y_{GT} &= -g_{m0} + jg_{m0} \omega 
\end{align*}
\]  

[1.39]

We note that the input impedance is very high (low $C_{gd}$) and the real part of the output admittance is close to $g_{m0}$; so it is adjustable by choosing the transistor grid width (grid development).

### 1.4.2. Cascade and cascode configurations

The studied configurations consist of the cascade of 2 two-port networks. It is possible to express the admittance matrix of the set according to these basic two-port networks and derive a Pi equivalent circuit (Figure 1.46).

![Pi equivalent circuit of a cascade of two two-port networks](image)

**Figure 1.46. Pi equivalent circuit of a cascade of two two-port networks**

The elements of the equivalent circuit are expressed in terms of those of basic two-port networks:

\[
\begin{align*}
Y_{Q1} &= Y_{A1} + Y_{A3} + Y_{AT} + Y_{A2} + Y_{B1} + Y_{B3} \\
Y_{Q2} &= Y_{B2} + Y_{B3} + Y_{BT} + Y_{A2} + Y_{A3} + Y_{B1} + Y_{B3} \\
Y_{Q3} &= Y_{A2} + Y_{A3} + Y_{B1} + Y_{B3} \\
Y_{QT} &= -\frac{Y_{AT} Y_{BT} - Y_{B2} Y_{AT} - Y_{AT} Y_{B3}}{Y_{A2} + Y_{A3} + Y_{B1} + Y_{B3}} \\
I_{NQ1} &= I_{NA1} + \frac{Y_{A3}}{Y_{A2} + Y_{A3} + Y_{B1} + Y_{B3}} (I_{NB1} + I_{NA2}) \\
I_{NQ2} &= I_{NB2} - \frac{Y_{BT} - Y_{B3}}{Y_{A2} + Y_{A3} + Y_{B1} + Y_{B3}} (I_{NB1} + I_{NA2})
\end{align*}
\]  

[1.40]
1.4.2.1. **Cascade configuration**

The circuit consists of two cascaded common-source configurations. Matrices \( Y_a \) and \( Y_b \) correspond to matrices \( Y_s \) and \( Y_s' \).

The simplified equivalent circuit elements are:

\[
\begin{aligned}
Y_{Q1} &= R_{gr1} C_{gr2} \omega^2 + jC_{gr1} \omega + jC_{gd1} g_{m01} + g_{d1} \frac{1 + \left( \frac{\omega}{\omega_1} \right)^2 - j \frac{\omega}{\omega_1}}{1 + \left( \frac{\omega}{\omega_0} \right)^2 - j \frac{\omega}{\omega_0}} \\
Y_{Q2} &= g_{d1} + jC_{ds2} \omega + jC_{gd2} g_{m02} + g_{d1} \frac{1 + \left( \frac{\omega}{\omega_3} \right)^2 - j \frac{\omega}{\omega_3}}{1 + \left( \frac{\omega}{\omega_0} \right)^2 - j \frac{\omega}{\omega_0}} \\
Y_{Q3} &= -C_{gd1} C_{gd2} \omega^2 \frac{1}{g_{d1} + \left( \frac{\omega}{\omega_0} \right)^2 - j \frac{\omega}{\omega_0}} \\
Y_{Q7} &= \frac{g_{m01} g_{m02}}{g_{d1}} \frac{1 - \left( \frac{\omega}{\omega_3} \right)^2 - j \frac{\omega}{\omega_3}}{1 + \left( \frac{\omega}{\omega_0} \right)^2 - j \frac{\omega}{\omega_0}}
\end{aligned}
\]  

\[1.41\]

\[
\begin{aligned}
\omega_0 &= \frac{g_{d1}}{C_{ds1} + C_{gd1} + C_{gr2}} & \omega_0'^2 &= \frac{g_{d1}}{R_{gr2} C_{gr2}} \\
\omega_1 &= \frac{g_{m01} + g_{d1}}{g_{m01} \tau_1 - C_{ds1} - C_{gd2}} & \omega_1'^2 &= \frac{g_{m01} + g_{d1}}{R_{gr2} C_{gd2}} \\
\omega_2 &= \frac{g_{m02} + g_{d1}}{g_{m02} \tau_2 - C_{ds2} - C_{gd1}} & \omega_2'^2 &= \frac{g_{m02} + g_{d1}}{R_{gr2} C_{gd1}} \\
\omega_3 &= \frac{g_{m01} g_{m02}}{g_{m01} g_{m02} \left( \tau_1 + \tau_2 \right) + g_{m02} C_{gd1} + g_{m01} C_{gd2}} & \omega_3'^2 &= \frac{g_{m01} g_{m02}}{g_{m01} g_{m02} \left( \tau_1 + \tau_2 \right) + g_{m02} \tau_2 C_{gd1} + g_{m01} \tau_1 C_{gd2}}
\end{aligned}
\]
An example of characteristics is shown in Figure 1.47, corresponding to two identical transistors.

There is a noticeable improvement of unilaterality, maximum gain and especially stability, since the circuit is unconditionally stable.

![Graphs showing performance characteristics](image)

**Figure 1.47. Performances of cascade mounting**

The main difficulty lies in the static polarization of each transistor, the most effective solution consisting of using complementary enhancement and depletion transistors, which avoids the use of a bond capacity between the two stages.
1.4.2.2. Cascode configuration

The circuit consists of cascading from a common-source configuration and a common-grid configuration. Matrix \( Y_A \) corresponds to matrix \( Y_s \) and matrix \( Y_a \) corresponds to the matrix \( Y'_C \).

\[
\begin{align*}
Y_{Q1} &= R_{g_s1}C_{g_s1}\omega^2 + jC_{g_s1}\omega + jC_{g_d1}\omega \frac{g_{m01} + g_{m02} + g_{d1}}{g_{m02} + g_{d1} + g_{d2}} \left( 1 + \frac{\omega}{\omega_1} \right)^2 - j \frac{\omega}{\omega_0} \\
Y_{Q2} &= jC_{g_d2}\omega + \frac{g_{d1}g_{d2}}{g_{m02} + g_{d1} + g_{d2}} \left( 1 - \frac{\omega}{\omega_3} \right)^2 + j \frac{\omega}{\omega_2} \left( 1 + \left( \frac{\omega}{\omega_1} \right)^2 \right) \left( 1 - \frac{\omega}{\omega_0} \right) \\
Y_{Q3} &= \frac{-C_{g_d1}C_{d2}\omega^3 + jg_{d2}C_{gd1}\omega}{\left( g_{m02} + g_{d1} + g_{d2} \right) \left( 1 - \frac{\omega}{\omega_0} \right)} \\
Y_{Q4} &= \frac{g_{m01}\left( g_{m02} + g_{d2} \right)}{g_{m02} + g_{d1} + g_{d2}} \left( 1 - \frac{\omega}{\omega_3} \right)^2 - j \frac{\omega}{\omega_5} \left( 1 - \frac{\omega}{\omega_0} \right)
\end{align*}
\]

\[ [1.42] \]

\[
\begin{align*}
\omega_0 &= \frac{g_{m02} + g_{d1} + g_{d2}}{g_{m02} \tau_2 - \left( C_{g_{s2}} + C_{d_{s2}} + C_{d_{s1}} + C_{d_{g1}} \right)} \\
\omega_1 &= \frac{g_{m01} + g_{m02} + g_{d1}}{g_{m01} \tau_1 + g_{m02} \tau_2 - \left( C_{g_{s1}} + C_{d_{s1}} \right)} \\
\omega_2 &= \frac{g_{d1}g_{d2}}{g_{d1}C_{d_{s1}} + g_{d2} \left( C_{g_{s2}} + C_{d_{s1}} \right)} \\
\omega_3 &= \frac{g_{d2}}{C_{d_{s1}} \left( C_{d_{s1}} + C_{g_{s2}} \right) - g_{d2}R_{g_{s2}}C_{g_{s2}}^2} \\
\omega_4 &= \frac{g_{m01} \left( g_{m02} + g_{d22} \right)}{g_{m01} \tau_1 \tau_2 + g_{m02} \tau_2 C_{d_{g1}} - g_{m01} \tau_1 C_{d_{s2}}} \\
\omega_5 &= \frac{g_{m01} \left( g_{m02} + g_{d22} \right)}{g_{m01} \tau_1 + \tau_2 + g_{m02} C_{g_{s1}} - g_{m01} C_{d_{s2}} + g_{m01} \tau_2}
\end{align*}
\]

with:

\[
\begin{align*}
\omega^2 &= \frac{g_{m01} + g_{m02} + g_{d1}}{R_{g_{s1}}C_{g_{s1}}^2} \\
\alpha^2 &= \frac{g_{d1}C_{d_{s2}} + g_{d2} \left( C_{g_{s2}} + C_{d_{s1}} \right)}{R_{g_{s2}}C_{d_{s2}}C_{g_{s2}}^2}
\end{align*}
\]
An example of characteristics is shown in Figure 1.48, corresponding to two identical transistors.

**Figure 1.48. Performance of the cascode configuration**

The output impedance can have a negative real part at high frequencies. A simple way to solve this problem is to place a feedback capacitor in the second stage grid. The results in Figure 1.48 correspond to a grounding grid or to the use of a 0.3 pF capacitor. The main advantage of this arrangement is, on the one hand, to improve the unilaterality and, on the other hand, to reduce the output conductance.
1.5. Wideband amplification

If we wish to increase the amplifier frequency band of operation, the question of impedance value choice of the transistor arises once again. The previous results in sections 1.2 and 1.3 concerning stability, noise factor and maximum power transfer are valid; they must simply be applied to the whole frequency band. Similarly, the stabilization and polarization techniques presented in these same sections are applicable by favoring those that show wideband behavior.

If we suppose a transistor is unconditionally stable and if the simultaneous matching is performed over the whole frequency band, then amplifier gain is equal to the maximum gain. The latter varies with the frequency on a slope of $-20\, \text{dB per decade}$, which means that the amplifier gain varies with frequency.

This poses a problem because the specifications of an amplifier usually require flat gain in the frequency band; we must then use methods to correct gain variation. The correction comprises the elimination of excess transmitted power at low frequencies (Figure 1.49).

![Figure 1.49. Maximum gain versus frequency](image)

Several solutions exist for this:

– Selective mismatching: excess power is reflected at the input and/or output. The result is an amplifier port mismatch, which limits the bandwidth or imposes more elaborate structures that are detailed in section 1.5.2.

– Selective dissipation: excess power is dissipated in resistors associated with reactive elements for varying power dissipation with frequency. Two solutions for this are detailed in sections 1.5.3 and 1.5.4.

– Specific structures for wideband amplification such as active matching and distributed amplification are presented in sections 1.5.5 and 1.5.6.
1.5.1. Reactive wideband matching

The issue of wideband impedance matching using purely reactive circuits resembles the one developed for narrowband circuits for which the properties are explained in sections 1.1.4 and 1.2.5.

The fundamental difference is due to the fact that it is impossible, on a given frequency band, to obtain a perfect match whatever the frequency. However, it is possible to obtain it for some frequency points and to ensure that its value is limited to the rest of the band.

1.5.1.1. Bode–Fano relations

These relations express the limit value that the reflection coefficient can take at the input of the matching circuit, according to the desired frequency band and the load impedance type.

\[
\Gamma(\omega) = \frac{Z_L - Z_0}{Z_L + Z_0},
\]

where:
- \( Q \) is the quality factor for load impedance;
- \( B_p \) is the relative bandwidth: \( B_p = (\omega_2 - \omega_1) / \omega_0 \);
- \( \Gamma_{\min} \) is the value of the reflection coefficient in the frequency bandwidth.

To better understand the significance of these relations, let us consider an ideal case where the reflection coefficient is constant in the frequency bandwidth:

\[
Q = \frac{\omega_0}{\omega_0}, \quad \Gamma(\omega) = \Gamma_{\min}, \quad \omega_0 = \omega_1 = \omega_2.
\]
The application of the relation for a low-pass-type impedance gives:

$$|\Gamma_{\text{min}}| = \exp\left(-\frac{\pi}{QB_p}\right)$$  \hspace{1cm} [1.43]

1.5.1.2. Synthesis of reactive two-port networks with wideband matching

There are many synthesis methods available for reactive two-port networks:
- real frequencies methods proposed in particular by Belevitch and Carlin;
- method using synthesis of transfer functions proposed by Ha.

The presentation of a detailed theory of these methods is beyond the scope of this book; however, references are provided at the end of the book for interested readers.

The problem is slightly different depending on whether the matching two-port network is input/output or interstage. In the first case, one of the impedances is real ($R_0 = 50 \, \Omega$), while in the second case, the two impedances are complex.

For example, let us develop a simple method based on the classical theory of bandpass filters using inductors and capacitors. The details of the calculation are presented in Appendix 4.

Initially, let us consider the case of input/output two-port networks. In this case, presenting $Z_2$ to port 2 when port 1 is closed by $R_0$ is the same as presenting $R_0$ to port 1 when port 2 is closed by $Z_2^*$ (Figure 1.50).

The objective will be to present the impedance $R_0$ to port 1 of the two-port network when port 2 is closed by the complex conjugate of the desired optimum impedance, for example $Z_{m1}^*$ for the maximum gain or $Z_{opt}^*$ for the minimum noise factor.
This impedance must be known as a series or parallel equivalent circuit.

The Bode–Fano relations show that the reflection coefficient at the input will at best be smaller than a limit value which depends on the frequency band and characteristics of the load impedance (Figure 1.51).

\[
\Gamma_E = \frac{Z_E - R_0}{Z_E + R_0}
\]

\[|\Gamma_E| \leq |\Gamma_{E_{\text{max}}}|\]

As two-port networks are lossless, minimizing the reflection coefficient is equivalent to maximizing the transfer coefficient.

\[|S_{21}|^2 = 1 - |S_{11}|^2 = 1 - |S_{22}|^2\]

We deduce a relation between reflection and transmission matching conditions as:

\[|S_{21 \min}|^2 = 1 - |S_{11 \max}|^2\]  \[1.44\]

In practice, the quantities used are:

– reflection coefficient in dB (return loss): \(RL_{(dB)} = 20 \log |S_{11 \max}|\);

– ripple transmission in dB: \(\text{Ripple}_{(dB)} = -20 \log |S_{21 \min}|\).

The table below shows some correspondence between these quantities for commonly used values.
Return Loss (dB) | $|S_{11}|$ | $|S_{21}|$ | Ripple (dB) \\
--- | --- | --- | --- \\
$-20dB$ | $0.1$ | $0.995$ | $0.043dB$ \\
$-15dB$ | $0.177$ | $0.984$ | $0.14dB$ \\
$-10dB$ | $0.316$ | $0.948$ | $0.46dB$

It is therefore possible to use the theory of filters based on classical approximation functions (Butterworth, Chebyshev, Bessel, etc.) after normalization of the pattern and transformation into a low-pass equivalent. Note that the pattern is limited to a ripple in the bandwidth and the filter order is an adjustable parameter available to the designer.

A ladder structure is obtained with $g_k$ coefficients, corresponding to normalized impedance or admittance.

This method is applicable, in the first instance, to a real impedance.

![Figure 1.52. Topology of the matching circuit](image)

Figure 1.52 shows the topology of a normalized filter, allowing us to get the right ripple in the desired frequency band. In the bandwidth, if the filter is closed by a normalized impedance equal to $g_{n+1}$, the normalized input impedance is close to 1, or by denormalizing an input impedance close to $R_{\text{norm}}$.
The \( R_{\text{norm}} \) filter normalization resistor is different from the reference resistor \( R_0 \); therefore, it is necessary to insert an ideal impedance transformer upstream of the filter for which the transformation ratio is 
\[
    n_T = \sqrt{\frac{R_0}{R_{\text{norm}}}}
\]  
(Figure 1.53).

![Figure 1.53. Introduction of an impedance transformer](image)

As the ideal impedance transformer does not exist in reality, it is necessary to eliminate it using the Darlington equivalence shown in Figure 1.54.

![Figure 1.54. Darlington equivalences](image)

These equivalences take different forms depending on the nature of the impedances associated with the transformer. In all cases, they are subject to validity conditions. Detailed results are shown in Appendix 4; an example of the result is...
given by the equations in 1.45 for the case of a series structure, impedance \( Z_1 \) being an LC series circuit and \( Z_2 \) an inductor.

\[
\begin{align*}
L_{T1} &= n_T^2 L_1 + n_T (n_T - 1)L_2 \\
C_{T1} &= \frac{C_1}{n_T^2} \\
L_{T2} &= (1 - n_T)L_2 \\
L_{T3} &= n_T L_2
\end{align*}
\]

validity condition: \( 1 > n_T > \frac{L_2}{L_1 + L_2} \) [1.45]

For a load impedance with a reactive part, the synthesis methodology consists of two stages:

– Design of a filter to match a resistor equal to the real part of the impedance. We therefore ignore the imaginary part. This design uses the Darlington equivalences, which are subject to conditions of validity (Appendix 4).

– Integration of the reactive part of impedance into the reactance of the last filter element. The load topology (series or parallel) imposes that of the last element of the filter and the physical feasibility criterion involves validity conditions for integration (Appendix 4).

\[ g_n g_{n+1} \geq QB \]

where \( Q \) is the quality factor for load impedance whose expression depends on the topology.

In Appendix 4, we show that the different validity conditions associated with the topology of the load and the reference impedance value \( R_0 \) limit the choice to four possibilities:

– Load impedance is a series circuit: \( R_{\text{norm}} = R_L g_{n+1} \) \( Q = \left. \frac{x_L}{r_L} \right|_{ob} \)

– \( R_0 < R_L g_{n+1} \) : the \( g_1 \) element is in series.
Amplification in Linear Mode

Feasibility conditions:

- The element is in parallel.

Feasibility conditions:

- The load impedance is a parallel circuit: \( R_{\text{norm}} = \frac{R_L}{g_{n+1}} Q = \frac{b_L}{g_L_{\text{leq}}} \)

- \( R_0 > R_L g_{n+1} \): the \( g_1 \) element is in parallel.

Feasibility conditions:

- \( R_0 < R_L g_{n+1} \): the \( g_1 \) element is in series.
- \( R_0 > R_L g_{n+1} \): the \( g_1 \) element is in parallel.

Feasibility conditions:

\[
\begin{align*}
1 + \frac{g_1 g_2}{B^2} & \geq \sqrt{\frac{R_0}{R_L}} g_{n+1} \geq 1 \\
g_{n+1} g_{n+1} & \geq Q_B
\end{align*}
\]

As an example, let us consider an RC-type series circuit to be matched on a frequency band of an octave. The data are the following:

\[
\begin{align*}
R_L &= 200 \Omega \\
C_L &= 0.1 pF \\
f_1 &= 4 \text{GHz} \\
f_2 &= 8 \text{GHz} \\
Q &= 1.407 \\
B &= 0.707 \\
\text{RL}_{\text{max}} &= -15 \text{dB} \\
Q_B &= 0.995
\end{align*}
\]

We choose a Chebyshev-type approximation function.

An RC series load type imposes a \( g_n \) element in series and \( R_0 < R_L g_{n+1} \) imposes a \( g_1 \) element in series. The filter order is therefore odd; in order to achieve a simple topology, we choose, for example, \( n = 3 \).

The values of the standard elements are \( g_1 = g_3 = 1.119 \quad g_2 = 1.154 \).

The validity conditions are met:

\[
g_3 > Q_B \quad 1 + \frac{g_1 g_2}{B^2} > \sqrt{\frac{R_L}{R_0}}
\]

It is therefore possible to integrate the imaginary part of the load into the last filter element and apply the Darlington equivalence to eliminate the impedance transformer. The topology as well as the simulation result is shown in Figure 1.55.

If the constraint on the reflection coefficient is more severe (e.g. \( \text{RL}_{\text{max}} = -20 \text{dB} \)), the \( g_3 \) coefficient decreases \( (g_3 = 0.853) \), and the integration condition is not achieved.
Similarly, the transformer elimination condition depends on the value of $R_L$ or the frequency bandwidth.

Interstage matching circuits are treated in the same way. Conditions for integration of impedance reactive elements must be respected at ports 1 and 2. An example with a second-order filter is shown in Figure 1.56.

![Figure 1.56. Example of interstage matching](image)

The presented method highlights the limitations that exist in the synthesis of matching networks that depend on frequency bandwidth and reflection coefficient limit value objectives. In practice, modern computer-aided design (CAD) software offers filter and performing matching circuit synthesis modules.
1.5.2. Selective mismatching

The principle is to provide port 1 and/or port 2 with different impedances from those that ensure maximum power transfer such that gain is constant in terms of frequency function. As matching two-port networks are lossless, reflection coefficients at the amplifier input and/or output are different from zero. Figure 1.49 shows that it is possible to apply matching conditions at the maximum frequency of band $f_M$ and increase the mismatch gradually until minimum frequency $f_m$.

Determining impedances to be presented to transistor ports can be done using constant gain circles for several frequency points in the desired frequency band.

This method enables low-noise wideband amplifiers to be designed by choosing the impedance presented at port 1 as the compromise between gain and noise factor, as shown in section 1.3.3.

The relation between gain loss and the reflection coefficient at input is given by relation [1.46]:

$$\left| \Gamma_{e1} \right|^2 = 1 - \frac{G_1}{G_{1\text{max}}}$$  \[1.46\]

The results of the application of this relation are given in the following table, which shows a rapid degradation of the reflection coefficient as a function of gain loss.

| $G_1/G_{1\text{max}}$ | $\left| \Gamma_{e1} \right|$ | TOS | Return Loss |
|-----------------------|-----------------|------|-------------|
| –0.1 dB               | 0.15            | 1.35 | –16.0 dB    |
| –0.5 dB               | 0.33            | 1.9  | –9.6 dB     |
| –1.0 dB               | 0.45            | 2.2  | –6.8 dB     |

This leads to a bandwidth limitation that is possible if we wish to limit the reflection coefficient degradation.

$$\alpha = \frac{f_M}{f_m} \Rightarrow \left( \frac{G_M}{G_m} \right)_{\text{dB}} = -6(\alpha - 1)$$

The following table shows the reflection coefficient at input depending on the relative bandwidth.
To improve the performance, gain loss can be allocated to amplifier input and output. For example, a bandwidth of 18% can be obtained with a gain loss of –0.6 dB at both ports, which limits the reflection coefficient value to about –9 dB.

Obtaining wider bandwidths leads to too high reflection coefficients. To overcome this drawback, more sophisticated topologies such as a balanced amplifier and a two-stage structure are required.

1.5.2.1. Balanced amplifier

The topology is identical to that presented in section 1.3.5 on low-noise amplifiers. It consists of using two identical amplifiers placed between two 3 dB 90° couplers (Figure 1.56).

![Figure 1.57. Balanced amplifier](image)

\[
S_{\text{ampl}} = \frac{1}{2} \begin{pmatrix} S_{B11} - S_{A11} & j(S_{A12} + S_{B12}) \\ j(S_{A21} + S_{B21}) & S_{A22} - S_{B22} \end{pmatrix}
\]

[1.47]

Identical amplifiers \( \Rightarrow S_{\text{ampl}} = \begin{pmatrix} 0 & jS_{12} \\ jS_{21} & 0 \end{pmatrix} \)
The equivalent amplifier between ports 1 and 2 therefore has the following properties:

– Input and output matching regardless of the amplifier reflection coefficients, provided that they are equal. It should be noted that power transfer is not improved, and the power reflected at the basic amplifier ports is simply directed toward ports 3 and 4, where it is dissipated in the matched loads.

– Power gain equal to that of a basic amplifier. The output power of each basic amplifier is halved, which improves the linearity of the device.

The main limitation of this type of amplifier is the bandwidth of directional couplers, which requires the use of wideband topologies such as the Lange coupler [PAS 05].

1.5.2.2. Multistage amplifier

This topology is based on the possibility offered by the third matching circuit. Input and output matching ensures maximum power transfer, which provides good reflection coefficients to the ports. The result is a drop of 12 dB in gain per octave, which can be compensated for by the interstage matching circuit. Impedances provided to each port of the latter can be obtained by using the available gain and constant power circles or by two-port network synthesis methods to obtain transfer parameters with a slope of 12 dB per octave.

A good unilaterality of transistors make easier the design of interstage circuits.

The advantages of this topology are:

– input–output matching;

– flat and higher gain because of the two stages.

The frequency bandwidths that can be obtained by this method are relatively limited (in the order of one octave) due to the synthesis of reactive two-port networks. Figure 1.58 summarizes the operational principles.

1.5.3. Resistive matching

The excess power transmitted (see Figure 1.49) is selectively dissipated in matching circuits placed at the input and output of the transistor. These must be dissipative and include at least one resistor in their topology.
The aim is to overcome the selective mismatch bandwidth limitations and target a very wide operating band of low-pass type.

Matching toward low frequencies has two difficulties:
– stability of the transistor;
– difficulty in designing a matching circuit.

The use of a resistor will help solve these two problems.

The presence of a resistor in the input matching circuit results in an increase in noise factor; this type of amplifier is therefore not suitable for low-noise amplifier design.

Let us describe the operation of two dissipative matching circuits before applying them to the design of a wideband amplifier.

1.5.3.1. Dissipative matching

Let us consider an RC series circuit (Figure 1.59).

Variation of the reflection coefficients as a function of frequency is given by equation [1.48]. Details of the calculation are provided in Appendix 5.

\[
\Gamma = \frac{1+(r-1)c.p}{1+(r+1)c.p} \quad [1.48]
\]
Matching at low frequencies can be easily done using a resistor in parallel. The resistor will also serve to stabilize the transistor. The circuit is shown in Figure 1.60 and the expression of the reflection coefficient is given by equation [1.49].

\[
\Gamma = \frac{1 - g_1 + (r - 1 - g_1) r c p}{1 + g_1 + (r + 1 + g_1) r c p}
\]

Analysis of this equation shows that low frequency matching is achieved with \( g_1 = 1 \) or \( R_1 = 50\Omega \). Under these conditions:

\[
\Gamma = \frac{-c p}{2 + (1 + 2 r) c p}
\]

The equation shows low frequency matching and degradation thereof as frequency increases.

To improve the frequency variation, we can modify the influence of the resistor with increasing frequency by adding an inductor in series as shown in Figure 1.61.

\[
\Gamma = \frac{L_1}{2 + L_1 (1 + 2 r) c p}
\]
The variation of the reflection coefficient is given by equation [1.50].

\[
\Gamma = \frac{(r_1 - 1) + (l_1 - r_1) + p + l_1 + c(r - 1)p^2}{(r_1 + 1) + (l_1 + 2r + c - r_1) + p + l_1 + c(r + 1)p^2}
\]  

[1.50]

This equation shows that it is possible to cancel the frequency variation of the first-degree numerator term, which can slow down the increase in reflection coefficient.

The optimum matching conditions are:

\[
\begin{align*}
R_1 &= R_0 \\
L_1 &= R_0^2 C
\end{align*}
\]  

[1.51a]

An additional improvement can be made by adding a cascaded inductor in series, as shown in Figure 1.62.

Expression of the reflection coefficient given by equation [1.51b] shows that it is possible to cancel the first- and second-degree numerator terms. A “maximally flat” type of response is obtained.

\[
\Gamma = \frac{(r_1 - 1) + (l_1 + I_2 - r_1) + p + [(l_1 + l_2)x + l_2 + r_1c - l_1c]p^2 + l_1 + l_2c.p^3}{(r_1 + 1) + (l_1 + l_2 + r_1) + p + [(l_1 + l_2)x + l_2 + r_1c + l_1c]p^2 + l_1 + l_2c.p^3}
\]  

[1.51b]

Optimum matching conditions are then written as:

\[
\begin{align*}
R_1 &= R_0 \\
L_1 &= R_0(R_0 + R) \frac{C}{2} \\
L_2 &= R_0(R_0 - R) \frac{C}{2}
\end{align*}
\]  

[1.52]
This equation shows that the second improvement is possible only if $R < R_0$.

Figure 1.63 shows the evolution of frequency variations of the reflection coefficient as a function of the matching circuit topology.

These variations are plotted as a function of normalized frequency $\frac{f}{f_{\text{norm}}}$ with

$$f_{\text{norm}} = \frac{1}{2\pi(R_0 + R)C}.$$ 

![Graph showing frequency variation of reflection coefficient](image)

**Figure 1.63. Frequency variation of the reflection coefficient: RC series circuit**

Improving the normalized frequency limit for a given maximum reflection coefficient is important. For example:

$$|\Gamma|_{\text{max}} = 0.2 \Rightarrow \frac{f}{f_{\text{norm}}}_{\text{max}} = \begin{cases} 0.5 & \text{1st topology} \\ 0.9 & \text{2nd topology} \\ 1.55 & \text{3rd topology} \end{cases}$$

An RC parallel circuit gives comparable results that are detailed in Appendix 5 and are summarized by equations [1.53].

1st topology: \[ r_i = \frac{1}{1-g} \Rightarrow R_i = \frac{R}{R-R_0} \text{ valid if } R > R_0 \]

2nd topology: \[ l_i = \frac{1}{1-g} \quad l_i = \frac{c}{(1-g)^2} \quad [1.53] \]
Amplification in Linear Mode

3rd topology: \[ r_1 = \frac{1}{1-g}, \quad l_1 = c \frac{\sqrt{1-g} - (1-g)}{g (1-g)^2}, \quad l_2 = c \frac{\sqrt{1-g}}{g} \]

Figure 1.64 shows the evolution of frequency variations of the reflection coefficient as a function of the matching circuit topology.

These variations are shown as a function of normalized frequency \[ \frac{f}{f_{\text{norm}}} \]
with

\[ f_{\text{norm}} = \frac{1}{2\pi(R_0 + R)C}. \]

Figure 1.64. Frequency variation of the reflection coefficient: RC parallel circuit

The results in terms of improving the bandwidth are comparable with those obtained for the RC series circuit.

1.5.3.2. Dissipative matching amplifier

Application to the design of a wideband amplifier is based on the use of a simplified model of the transistor. In particular, the transistor is assumed to be unilateral (Figure 1.65).

Figure 1.65. Simplified model of the field-effect transistor
Input and output matching can be obtained using the two circuits shown in section 1.5.3.1. The topology is shown in Figure 1.66.

![Amplifier topology](image)

**Figure 1.66. Amplifier topology**

Gain value at low frequency in the matching conditions is given by equation [1.54]:

\[
|S_{21}|_0 = \frac{g_m Z_0}{2}
\]  

[1.54]

This equation shows a minimum value for transconductance of the transistor in order to obtain gain.

\[
\frac{g_m Z_0}{2} > 1 \Rightarrow g_m > \frac{2}{Z_0} \Rightarrow g_m > 40 \text{ mSie} \quad \text{for} \quad Z_0 = 50 \Omega
\]

A gain of 10 dB requires a transconductance of 126 mSie.

For example, let us consider a transistor for which the simplified equivalent unilateral diagram elements are:

\[
\begin{cases}
  g_m = 120 \text{ mSie} \\
  R_G = 10 \Omega \\
  C_G = 0.4 \text{ pF} \\
  g_d = 2 \text{ mSie} \\
  C_D = 0.1 \text{ pF}
\end{cases}
\]

The simulation results of performances for different topologies are shown in Figure 1.67.

This method provides a good basis for optimizing results using CAD software to consider a more complete model of a transistor.
Figure 1.67. *Example of the performance of an amplifier with resistive matching*

1.5.4. **Feedback amplifier**

The topology consists of a transistor to which a feedback is applied, using impedance. Among all the possibilities of well-known feedbacks, the most widely used feedback is the parallel feedback; we will restrict our presentation to this solution.

Two approaches can be used to design a wideband feedback amplifier. The first approach is of the low-pass type and consists of searching for a feedback impedance for minimizing reflection coefficients for the two ports at low frequencies and increasing the cutoff frequency. The second approach, which is of the bandpass type, relies on a graphic method for determining the impedance such that maximum transducer power gain of the transistor is constant across the frequency band; it then remains to design non-dissipative matching circuits to present the impedances that lead to simultaneous complex conjugate matching (section 1.5.1).

The presence of a resistor in the feedback impedance degrades the noise factor increasingly with lower value. This topology is not suitable for designing a very low noise amplifier, but is suitable for average noise factors.

The feedback topology significantly improves the linearity of the amplifier.
1.5.4.1. Low-pass type amplifier

The determination of feedback is based on a simplified unilateral equivalent circuit such as the one shown in Figure 1.65. The feedback impedance is a resistor, and grid resistor (Figure 1.68) is neglected. Details of the calculation are given in Appendix 6.

![Parallel feedback diagram](image)

**Figure 1.68. Parallel feedback**

The scattering parameters are expressed as:

$$ S_{11} = \frac{1 + Z_0 g_d - Z_0 g (g_m + g_d) - Z_0 C_i p (1 + g + Z_0 g_d) - Z_0 C_p (1 + g) p - Z_0^2 C_i C_p p^2}{1 + Z_0 g_d + g[2 + Z_0 (g_m + g_d)] + Z_0 C_i p (1 + g + Z_0 g_d) + Z_0 C_p (1 + g) p + Z_0^2 C_i C_p p^2} $$

$$ S_{22} = \frac{1 - Z_0 g_d - Z_0 g (g_m + g_d) - Z_0 C_i p (1 + g + Z_0 g_d) - Z_0 C_p (1 + g) p - Z_0^2 C_i C_p p^2}{1 + Z_0 g_d + g[2 + Z_0 (g_m + g_d)] + Z_0 C_i p (1 + g + Z_0 g_d) + Z_0 C_p (1 + g) p + Z_0^2 C_i C_p p^2} $$

$$ S_{21} = \frac{-2 (Z_0 g_m - g)}{1 + Z_0 g_d + g[2 + Z_0 (g_m + g_d)] + Z_0 C_i p (1 + g + Z_0 g_d) + Z_0 C_p (1 + g) p + Z_0^2 C_i C_p p^2} $$

Low frequency matching at both ports leads to the following conditions:

$$ 1 + Z_0 g_d - Z_0 g (g_m + g_d) = 0 $$

$$ 1 - Z_0 g_d - Z_0 g (g_m + g_d) = 0 $$

Simultaneous matching is only possible if $Z_0 g_d << 1$.

Under these conditions:

$$ g = \frac{1}{Z_0 (g_m + g_d)} \Rightarrow R = Z_0^2 (g_m + g_d) \quad [1.55] $$

If $Z_0 g_d$ is not low enough, equation [1.55] is still used, but in this case reflection coefficients at the ports are no longer zero at low frequency.

$$ |S_{11}|_0 = |S_{22}|_0 = \frac{Z_0 g_d (g_m + g_d)}{2 + Z_0 (g_m + g_d) (2 + Z_0 g_d)} $$
For example, let us consider the transistor used in section 1.5.3.2 for which
\[
\begin{align*}
g_m &= 120 \text{ mS} \\
g_d &= 2 \text{ mS}
\end{align*}
\]
and \( Z_0 = 50 \Omega \). Thus, we deduce that \( R = 305 \Omega \).

In this example, \( Z_0 g_d = 0.1 \); therefore, \( |S_{11}|_0 = |S_{22}|_0 \approx 0.05 \), which is a perfectly acceptable value.

Low frequency gain is written as:
\[
S_{210} = -\frac{2\left(Z_0^2 g_m (g_m + g_d) - 1\right)}{2 + Z_0 (g_m + g_d) (2 + Z_0 g_d)}
\]

These equations are simplified if \( g_m \gg g_d \) and \( Z_0 g_d << 2 \).

Again of 10 dB requires a transconductance of 83 mS.

Figure 1.69 shows the simulation results of resistive feedback using the simplified model of a transistor.

There is a clear improvement of the reflection coefficient as well as a decrease in the low-frequency gain.

The gain variation is of the second-order low-pass type. The simplified expression of cutoff frequency is:
\[
\omega_0^2 = \frac{2(1 + Z_0 g_m)}{Z_0^3 g_m C_g C_D}
\]
To improve the bandwidth, several solutions are described in Appendix 6:

– One solution is to use an inductor in series with the feedback resistor, which does not simultaneously improve the input and output matching. Figure 1.70 shows the simulation results compared to those of the feedback resistor alone. An improvement in the bandwidth for gain and input matching can be seen, but there is a degradation in the output matching.
– Another solution is to increase the transistor output capacitor. Figure 1.71 shows the simulation results compared to those of the feedback resistor alone. An improvement in the bandwidth for the gain and input and output matching can be seen, however it still remains quite low.

![Figure 1.71. Improvement of the bandwidth: capacitor in parallel](image1)

– A final solution is to use two inductors. Figure 1.71 shows the simulation results when compared to those of the resistive feedback alone. There is an improvement in the bandwidth for the gain and the input and output matching.

![Figure 1.72. Improvement of the bandwidth: two inductors](image2)
1.5.4.2. Bandpass-type amplifier

Determination of feedback impedance aims to obtain maximum transfer gain of the transistor, constant across the frequency band. We deduce the optimum impedances to obtain complex conjugate matching that is simultaneous upon input and output. It then remains to design non-dissipative matching circuits for presenting these impedances to the transistor ports.

Feedback impedance can be obtained in several ways:

– Use of CAD software giving the value of $G_{T_{\text{max}}}$ and an optimization algorithm to obtain a constant value over a given frequency band. This approach provides good results but has the drawback of assuming a priori feedback impedance topology.

– Use of a graphical method to trace the points of the feedback impedance plane providing a determined gain. We will detail this approach, which has the advantage of not assuming a topology for feedback impedance.

In Appendix 7, it is shown that the set of points in the complex plane, corresponding to the reflection coefficient of the feedback impedance, is a family of circles for which the useful portion is limited by unconditional stability. The envelope of these circles corresponds to the curve $K_T = 1$.

Figure 1.73 gives an example of a circle plot at constant maximum gain for an HEMT-type transistor at a frequency of 10 GHz.

![Figure 1.73. Constant maximum gain circles](image)

Determining feedback impedance is done by plotting the circle corresponding to a given gain for several frequencies in the desired operating band. An example is shown in Figure 1.74 for a gain of 10 dB and three frequencies: 10, 20 and 30 GHz.
A possible topology for feedback impedance is an RLC series circuit with

\[
\begin{align*}
R &= 165\Omega \\
L &= 1.3nH \\
C &= 5pF
\end{align*}
\]

Figure 1.75 gives the simulation result showing a maximum gain of 10 dB.

It is then possible to determine optimal impedances for combined matching with the two ports. The results are shown in Figure 1.76.
These impedances can be represented by RLC parallel circuits. The reactive two-port networks for matching both ports over the desired frequency band by one of the methods described in section 1.5.1.2 remain to be determined.

1.5.5. Active matching amplifier

This wideband matching technique is based on properties of common-grid and common-drain topologies, which have been discussed in section 1.1.4.

The input impedance of the common-grid configuration and the output impedance of the common-drain configuration can be adjusted through transistor transconductance value.
The topology of the amplifier therefore consists of cascading three transistors: the first in common-grid configuration, which provides input matching; the second in common-source configuration, which provides gain; and the third in common-drain configuration for output matching.

If an input and output impedance equals $50\,\Omega$, the transconductance value should be $g_m = 20\,mS\,\text{Sie}$, and it can be adjusted by choosing the transistor grid width or the grid polarization. The transconductance value of the common-source transistor determines the gain of the amplifier.

To obtain flat gain, it is necessary to apply parallel feedback on the common-source stage, as described in section 1.5.4.

The noise factor is close to that of the common-grid stage.

Figure 1.77 shows the simulation results of an active matching low-pass type amplifier with a gain of 10 dB and a cutoff frequency of about 20 GHz. The transconductance of the common-source configuration is 120 mS\,\text{Sie}. The feedback circuit consists of a 350 \,\Omega resistor, a 1.7 nH inductor and a 20 \,\text{pF} capacitor.

![Figure 1.77. Active matching amplifier](image)
1.5.6. Distributed amplifier

The topologies described in the preceding sections consist of cascading two-port networks, therefore approximately multiplying their gains.

The principle of the distributed amplifier is different in that it uses active coupling with the help of the transistor between two transmission lines, which may have distributed constants.

Obtaining gain is based on the adjustment of propagation constants of transmission lines to generate constructive couplings between signals.

1.5.6.1. Principle of the distributed amplifier

The presented topology uses field-effect transistors and lumped elements. It is easily transposable to the distributed transmission lines and bipolar transistors.

The input and output transmission lines are generated by inductors associated with the transistor capacitors.

![Figure 1.78. Principle of the distributed amplifier](image)

Simplified operation analysis can be performed by considering a unilateral equivalent circuit of the transistor such as the one shown in Figure 1.65. The equivalent circuit of the amplifier becomes the one shown in Figure 1.79.

The grid and drain lines are formed by cascading T-symmetrical cells.

These cells can be represented by their characteristic impedance \( Z_{0G} \) or \( Z_{0\bar{G}} \) and the characteristic propagation parameter \( \theta_G = \alpha_G + j\beta_G \) or \( \theta_D = \alpha_D + j\beta_D \) (see Figure 1.80). The theory of these parameters is discussed in [GAU 07].
Amplification in Linear Mode

**Figure 1.79. Simplified equivalent circuit of the amplifier**

\[ Z = \begin{pmatrix} \frac{Z_1}{2} + Z_2 & Z_1 \\ Z_2 & \frac{Z_1}{2} + Z_2 \end{pmatrix} \]

\[ Z_0 = \sqrt{Z_1 Z_2} \left[ \frac{1 + Z_2}{4Z_2} \right] \]

\[ \cosh \theta = \frac{1 + \frac{Z_1}{Z_2}}{2Z_2} \]

\[ \sinh \theta = \frac{\sqrt{Z_1}}{4Z_2} \]

\[ Z_2 = \frac{Z_0}{\sinh \theta} \]

**Figure 1.80. T-symmetrical cells**

1.5.6.2. Analysis of grid and drain lines

The grid line is shown in Figure 1.81.

**Figure 1.81. Grid line**

It is loaded at output by an impedance equal to its characteristic impedance \( Z_{0G} \); the input impedance of each cell is therefore equal to \( Z_{0G} \).

The amplification voltage of each cell is easily expressed in terms of the characteristic propagation factor \( \theta_G \).

\[ \frac{V_2^{(k)}}{V_1^{(k)}} = e^{-\theta_0} \Rightarrow \frac{V_2^{(k)}}{V_1^{(k)}} = e^{-\theta_0} \]
We can deduce the value of the transistor grid voltage of cell \( k \) based on the line input voltage. Details of the calculation are presented in Appendix 8.

\[ v_G^{(k)} = \frac{\theta}{\sin \left( \frac{\theta}{2} \right)} e^{-K_s \theta} \cdot v_1^{(i)} \]  

[1.57]

Propagation characteristics for the grid line are explained in Appendix 8 for general cases. They are simplified in two special cases:

\[
R_G = 0 \text{ and } \omega << \omega_{0G} \implies \begin{cases} 
\alpha_G = 0 \\
\beta_G = 2 \frac{\omega}{\omega_{0G}}
\end{cases} \text{ with } \omega_{0G} = \frac{2}{\sqrt{L_G C_G}}
\]

\[
R_G \text{ low losses and } \omega << \omega_{0G} \implies \begin{cases} 
\alpha_G = \frac{\omega^2}{\omega_G \omega_{0G}} \\
\beta_G = 2 \frac{\omega}{\omega_{0G}}
\end{cases} \text{ with } \omega_G = \frac{1}{R_G C_G}
\]

The drain line is shown in Figure 1.82.

![Drain line diagram](image)

**Figure 1.82. Drain line**

It is loaded at both ports by an impedance equal to its characteristic impedance \( Z_{0D} \); the input and output impedance of each cell is therefore equal to \( Z_{0D} \).
The control voltage of the current generator is different from the grid voltage applied to the transistor; the value of $g_m$ is, therefore, different from that of the transistor $g_{m0}$:

\[ g_m = \frac{g_{m0}}{1 + j \frac{\omega}{\omega_G}} \]

As the line is matched at output, we can write:

\[ \frac{v^{(n)}_2}{v^{(k)}_2} = e^{-(n-k)\theta_0} \]

This suggests a relation between the output voltage of cell $k$ and the control voltage thereof (Appendix 8):

\[ v^{(k)}_2 = -g_m Z_{0D} v^{(k)}_G e^{\frac{\theta_0}{2}} 2.ch\left(\frac{\theta_D}{2}\right) \]

We can deduce the output voltage of the drain line based on the control voltage of cell $k$.

\[ v^{(n)}_2 = e^{-(n-k)\theta_0} v^{(k)}_2 = -g_m Z_{0D} e^{\frac{\theta_0}{2}} e^{-(n-k)\theta_0} v^{(k)}_G 2.ch\left(\frac{\theta_D}{2}\right) \]  \[ \text{[1.58]} \]

The propagation characteristics of the drain line are explained in Appendix 8 for general cases. They are simplified in two special cases:

\[ g_d = 0 \text{ and } \omega \ll \omega_{0D} \Rightarrow \left\{ \begin{array}{l}
R_{0D} = \frac{L_D}{\sqrt{C_D}} \\
\alpha_D = 0 \quad \text{with} \quad \omega_{0D} = \frac{2}{\sqrt{L_D C_D}} \\
\beta_D = 2 \frac{\omega}{\omega_D}
\end{array} \right. \]
Low losses and $\omega \ll \omega_D \Rightarrow$

$$R_{0D} = \frac{L_D}{C_D}$$

$$\alpha_D = \frac{\omega_D}{\omega} \quad \text{with} \quad \omega_D = \frac{g_d}{C_D}$$

$$\beta_D = 2 \frac{\omega}{\omega_D}$$

1.5.6.3. Operation of the amplifier

The input voltage of the amplifier is: $V_E = V_1^{(1)}$ grid line.

The output voltage of the amplifier is: $V_S = \sum_{k=1}^{k=N} V_2^{(n)}$ drain line.

Thus, substituting with equations [1.57] and [1.58], we get:

$$V_S = -g_m Z_{0D} \frac{e^{\theta_0 - \theta_0}}{2ch\left(\frac{\theta_G}{2}\right)ch\left(\frac{\theta_D}{2}\right)} e^{-n(\theta_0 - \theta_0)} \sum_{k=1}^{k=N} e^{-k(\theta_0 - \theta_0)} V_E$$

In Appendix 8, we show that this equation can be written in the following form, which represents the voltage gain of the amplifier:

$$\frac{V_S}{V_E} = -g_m Z_{0D} \frac{sh\left(\frac{n(\theta_G - \theta_D)}{2}\right)}{ch\left(\frac{\theta_G}{2}\right)ch\left(\frac{\theta_D}{2}\right)sh\left(\frac{\theta_e - \theta_D}{2}\right)} e^{-n(\theta_0 + \theta_0)}$$

[1.59]

The power gain is easily determined:

- Input power: $P_E = \frac{|V_E|^2}{2\Re(Z_E)} = \frac{|V_E|^2}{2\Re(Z_{0G})}$

- Output power: $P_S = \frac{|V_S|^2}{2\Re(Z_S)} = \frac{|V_E|^2}{2\Re(Z_{0D})}$
Thus:

\[
G_p = \frac{\Re(Z_{0G})}{\Re(Z_{0D})} \left| \frac{g_m}{Z_{0D}} \right|^2 \left[ \frac{\sin^2 \left( \frac{\theta_G - \theta_D}{2} \right)}{(1 + \cos \theta_G)(1 + \cos \theta_D)} \right]^2 e^{-n(\alpha_G + \alpha_D)}
\]

To understand the operating conditions of the amplifier, let us consider the simple case of lossless lines:

\[
\begin{cases}
R_G = 0 \\
g_D = 0
\end{cases} \Rightarrow \begin{cases}
\alpha_G = \alpha_D = 0 \\
\theta_G = j\beta_G \\
\theta_D = j\beta_D \\
Z_{0G} = Z_{0D} = R_{0G}
\end{cases}
\]

and \( g_m = g_{m0} \)

The expression of power gain is simplified to:

\[
G_p = \frac{g_{m0}^2 R_{0G} R_{0D}}{(1 + \cos \beta_G)(1 + \cos \beta_D)} \left[ \sin \left( \frac{\beta_G - \beta_D}{2} \right) \sin \left( \frac{\beta_G + \beta_D}{2} \right) \right]^2
\]

We note that gain reaches a maximum if \( \beta_G - \beta_D = 0 \).

This means that the fundamental condition of operation will have equal propagation velocities on the grid and drain lines.

\[
\beta_G = \beta_D = \beta \Rightarrow G_p = \frac{g_{m0}^2 R_{0G} R_{0D}}{(1 + \cos \beta)^2}
\]

The value of gain at low frequency is:

\[
G_{p0} = \frac{g_{m0}^2 R_{0G} R_{0D}}{4} n^2
\]

If we consider the losses with equal phase velocities \( \beta_G = \beta_D = \beta \), then gain is written as:

\[
G_p = \frac{R_{0G} |Z_{0D}| \left| \frac{g_m}{Z_{0D}} \right|^2}{R_{0D}} \left[ \frac{1}{(ch\alpha_G + \cos \beta)(ch\alpha_D + \cos \beta)} \right]^2 \left( \frac{\sin \left( \frac{\alpha_G - \alpha_D}{2} \right)}{\sin \left( \frac{\alpha_G + \alpha_D}{2} \right)} \right)^2 e^{-n(\alpha_G + \alpha_D)}
\]
Gain is no longer proportional to the square of the number of cells; there is an optimal number of cells above which the gain no longer increases:

\[ n_{opt} = \frac{\ln(\alpha_D) - \ln(\alpha_G)}{\alpha_D - \alpha_G} \]

Operating conditions can be summarized as follows:

\[ R_{bg} = \sqrt{\frac{L_G}{C_G}}, \quad \alpha_{bg} = \frac{1}{\sqrt{L_G C_G}} = \frac{1}{Z_{bg} C_G} \quad \text{and} \quad R_{bd} = \frac{L_D}{C_D}, \quad \alpha_{bd} = \frac{1}{\sqrt{L_D C_D}} = \frac{1}{Z_{bd} C_D} \]

or:

\[ \alpha_{bg} = \alpha_{bd} \Rightarrow R_{bg} C_G = R_{bd} C_D \]

\[ L_G = R_{bg}^2 C_G, \quad L_D = R_{bd}^2 C_D \]

If \( R_{bg} = R_{bd} = Z_0 \Rightarrow L_G = L_D \quad \text{and} \quad C_G = C_D. \]

The value of capacitors is imposed by the transistor. In practice, \( C_G > C_D \); therefore, it is necessary to ensure the equality of these capacitors.

Two solutions are possible for this:

– adding a \( C_{AD} \) capacitor such as \( C_{AD} + C_D = C_G \) in parallel between the drain and source;

– adding a \( C_{AG} \) capacitor such as \( \frac{1}{C_{AG}} + \frac{1}{C_G} = \frac{1}{C_D} \) in series with the grid transistor.

Among the many improvements to the basic topology proposed in the literature, we can note the replacement of a transistor by a cascode structure, which has the dual benefit of improving unilaterality and decreasing output conductance and thus reducing drain line losses.

Figure 1.83 shows an example of the result of a distributed amplifier with three cells with and without losses.

1.6. Differential amplifier

Many devices such as balanced mixers require the use of electrical quantities in the opposite phase; others, for technological reasons such as coupling in the silicon substrate of monolithic circuits, find an advantage in differential operation. Under these conditions, the study of differential amplifier function is of interest.
1.6.1. Four-port network with a plane of symmetry

The differential analysis of a four-port network can be performed using the theory of mixed modes.

Operation is assumed to be differential between ports 1 and 3 as the input and ports 2 and 4 as the output.

Let us use the mixed-mode theory applied to admittance parameters; similar analog results are obtained with impedance and scattering parameters. Details of the calculation are provided in Appendix 9.

The vectors of the voltages and currents of mixed modes are linear combinations of voltages and currents at the ports; they are obtained using the transformation matrix:

\[
M = \begin{pmatrix}
1 & 0 & -1 & 0 \\
0 & 1 & 0 & -1 \\
1 & 0 & 1 & 0 \\
0 & 1 & 0 & 1 \\
\end{pmatrix}
\Rightarrow V_M = M V \text{ and } I_M = M I
\]

These mixed-mode vectors can be written in the form of two subvectors:

- differential mode: \( V_d = \begin{pmatrix} V_{M1} \\ V_{M2} \end{pmatrix} = \begin{pmatrix} V_1 - V_3 \\ V_2 - V_4 \end{pmatrix} \)
We define a mixed-mode admittance matrix and a mixed-mode noise-current vector:

\[
Y_M = M.Y.M^{-1}
\]

\[
I_{NM} = M.I_N \Rightarrow C_{YM} = I_{NM}^*I_{NM}^* = M.C_Y.M^*
\]

Mixed-mode operation is then described by:

\[
\begin{pmatrix}
I_d \\
I_c
\end{pmatrix} = \begin{pmatrix}
Y_{dd} & Y_{dc} \\
Y_{cd} & Y_{cc}
\end{pmatrix}\begin{pmatrix}
V_d \\
V_c
\end{pmatrix} + \begin{pmatrix}
I_{Nd} \\
I_{Nc}
\end{pmatrix}
\]

Each submatrix is characteristic of differential-mode and common-mode operations for diagonal terms and coupling between these modes for non-diagonal terms.

If the four-port network has a plane of symmetry, as shown in Appendix 9, the coupling submatrices are zero and noise subvectors are non-correlated.

\[
Y_M = \begin{pmatrix}
Y_{dd} & 0 \\
0 & Y_{cc}
\end{pmatrix}, \quad C_{YM} = \begin{pmatrix}
C_{Ydd} & 0 \\
0 & C_{Ycc}
\end{pmatrix}
\]

In this case, the analysis of four-port network operation can be replaced by the study of two independent two-port networks:

– Differential mode for which excitation voltages at symmetrical ports are of equal amplitude and are in phase opposition. Under this situation, operating conditions are unchanged if the symmetry plane is replaced by a short-circuit plane. This configuration defines the two-port network in differential mode.

– Common mode for which excitation voltages of symmetrical ports are of equal amplitude and are in phase. Under this situation, operating conditions remain unchanged if we replace the plane of symmetry by an open-circuit plane. This configuration defines the two-port network in common mode.

### 1.6.2. Differential amplifier

The operation of a four-port network in pure differential mode is performed when the transmission coefficient in common mode is zero (see Appendix 9).
\[ Y_{ce21} = Z_{ce21} = S_{ce21} = 0 \]

The most common amplifier topology consists of two transistors coupled by their source (or emitter). Coupling is performed by an impedance such as the one shown in Figure 1.84, where polarization circuits are not represented.

![Figure 1.84. Basic topology of a differential amplifier](image)

This topology contains a plane of symmetry; it is possible to decompose it into 2 two-port networks corresponding to differential and common modes as shown in Figure 1.85.

![Figure 1.85. Differential mode and common mode](image)

To determine the coupling impedance, we need to perform an approximated calculation using a simplified equivalent circuit such as the one shown in Figure 1.43.

The cancellation condition of common-mode transmission is simply expressed with impedance parameters:
which can be rewritten in terms of admittances parameters:

\[
Z_{dd/21} = \frac{Y_{dd/21}}{\Delta Y_d} \Rightarrow Y_{SC} = \frac{1}{Z_{SC}} = \frac{\Delta Y_d}{Y_{dd/21}}
\]

Assuming the frequency is low enough, the value of the coupling admittance can be written as:

\[
Y_{SC} = \left( \tau C_g + \frac{g_d}{g_m} R_{gs} C_g^2 - \frac{C_{gb} C_{gd} + C_{gb} C_{ds} + C_{gd} C_{ds}}{g_m} \right) \omega^2 + j \left( C_{gd} + \frac{g_d}{g_m} \left( C_{gb} + C_{gd} \right) \right) \omega
\]

This equation shows that optimum admittance consists of the parallel connection of a capacitor and a conductance for which the value may be negative and varies as the square of frequency. The latter is not physically feasible, so cancellation of common-mode transmission cannot be performed perfectly. To describe the quality of operation in differential mode, the notion of a common-mode rejection ratio (CMRR), which is defined as the ratio between the transmission coefficient in differential mode and common mode, is used. It may take on different expressions depending on the formalisms used:

\[
TMRC_{dB} = 20 \log \left( \frac{Y_{dd/21}}{Y_{cc/21}} \right) \text{ or } 20 \log \left( \frac{Z_{dd/21}}{Z_{cc/21}} \right) \text{ or } 20 \log \left( \frac{S_{dd/21}}{S_{cc/21}} \right)
\]

Figure 1.86 shows the CMRR variation for coupling impedances composed of a capacitor in parallel with a resistor of variable value. Deterioration at low frequency is directly related to the value of the resistor; a good rejection requires a high-value resistor which is not suitable for static polarization due to excessive consumption. To overcome this disadvantage, we can use the following solutions:

– Replace the resistor with an inductor: this solution allows narrowband-type operation.

– Use a transistor mounted as a current source: this solution limits static power dissipation but requires a transistor whose output conductance is low (\( R = 200 \ \Omega \)) in Figure 1.86).

– Replace the transistor with a cascode to complete the current source: the output conductance is very low and deteriorates the rejection very little at low frequency (\( R = 4000 \ \Omega \) in Figure 1.86).
A more general approach to improve the CMRR is to consider the particular role of the elements placed in the plane of symmetry that are only involved in common-mode transmission. Improvement of the CMRR can therefore be done using the following methodology:

– Increase transmission in differential mode by using matching circuits such as those described in the preceding sections.

– Minimize common-mode transmission by placing elements to reduce the gain in the plane of symmetry, as shown in Figure 1.87. Impedance topologies $Z_{DC}$ and $Z_{GC}$ make it possible to adjust the CMRR frequency response.

**Figure 1.87. Using the plane of symmetry**
For example, Figure 1.88 shows the topology of an amplifier using double-stub matching circuits. Each stub is closed in common mode by a component causing it to resonate.

![Diagram of a differential circuit](image)

**Figure 1.88. Example of a differential circuit**

- The active elements of the differential amplifier shown in Figure 1.88 consist of a cascade-type association of two field-effect transistors. This structure provides more gain and improves the stability (see section 1.4.2.1). The $T_1$ transistor is at “normally on” depletion while $T_2$ is at “normally off” enhancement; this allows us to use a positive $V_{gs2}$ control voltage, which facilitates the polarization of $T_2$:

- Polarization: the $V_{g1}$ voltage ensures polarization of the $T_1$ grid. Access is via stubs from the $Q_{in}$ matching two-port network. The $V_{d2}$ voltage ensures polarization of $V_{ds1}$ and $V_{gs2}$. Resistor $R$ is used to adjust the value of the source potential of transistor $T_2$. The $V_{d3}$ voltage ensures polarization of $V_{ds2}$. Access to $V_{ds2}$ and $V_{d3}$ is via quarter-wave lines. The $R_{stab}$ and $C_{stab}$ elements added to polarization port $V_{ds2}$ ensure the unconditional stability of the device regardless of frequency (see section 1.2.4).
– Matching networks $Q_{in}$ and $Q_{out}$: input and output amplifier impedance matching in differential mode is performed with a topology of two short stubs terminated by a short-circuit imposed by the plane of symmetry. The performances of the amplifier in differential mode are shown in Figure 1.89(a).

– Common-mode rejection ratio: to improve the CMRR of the amplifier, in addition to the conventional coupling impedance $Z_{ac}$, add $C_{res1}$, $C_{res2}$ and $C_{res3}$ capacitors at the end of stubs in the plane of symmetry of the structure such that they have no action in differential mode. The values of these capacitors are adjusted to induce a short circuit at the input of each stub. The resonant frequencies of each stub are selected to optimize the common-mode rejection frequency band. In the example presented in Figure 1.88, the input stub resonates at the central frequency and the two output stubs resonate at frequencies on both sides thereof. Common-mode gain then drops sharply at these frequencies, which significantly improves the CMRR in the bandwidth. The CMRR curves are shown in Figure 1.89(b). The results clearly show an improvement of the latter progressively as $C_{res1}$, $C_{res2}$ and $C_{res3}$ elements are added.

![Figure 1.89. Performance of the differential amplifier: a) in differential mode, b) common-mode rejection rate](image)

1.7. Bibliography


Amplification in Linear Mode


