

# Preface

As one looks over the history of electronics, it becomes clear that one of the primary reasons for major shifts in technology has been the requirement to move toward a more energy efficient operation as the level of complexity increases. This resulted in the movement from vacuum tubes to solid state-logic, from bipolar to MOS and most recently from NMOS to CMOS. Again, however, history is repeating itself and as the complexity of CMOS circuits increases, the issues of power and energy consumption are once again becoming critical. Fortunately, the energy expended per operation for CMOS is continually improving as the technology is advanced. Particularly helpful is the dramatic improvement in energy efficiency that is obtained by reducing the supply voltage, and many of the techniques that are presented in this book exploit that characteristic. However, voltage scaling alone is not enough as the complexity increases and as applications which require the use of a portable energy source require further energy reductions. This book describes a number of these strategies which range over all levels of the design process from optimization of the underlying CMOS technology, logic styles, circuit topologies and architectures, up to the applications and algorithms which are being executed.

The most significant development at the CMOS technology level for low-voltage systems is the reduction of the device threshold voltage. For continuously operated circuits, the increased leakage due to reduced threshold voltages is typically not significant. However, for “event-driven” computation in which intermittent computation activity triggered by external events is separated by long periods of inactivity (e.g., X-server), leakage power is critical. To satisfy the contradicting requirements of high performance during active periods and low-standby leakage, several device technologies and circuit styles have been developed. This includes the dynamic control of threshold voltages in triple-well CMOS using backgate effect, Multiple Threshold CMOS, variable threshold CMOS, and dual-gated SOI technology. All these technologies (Part II) provide a knob to reduce leakage power during idle periods while enabling low-threshold, high-speed operation during active periods.

As supply levels scale into the sub-1V regime exploiting emerging technologies and efficient architectures, there is a need for high-efficiency, low-power DC-DC conversion. In many cases, embedding the power supply control in the processor can save significant power. Rather than designing a system with a static supply to meet a specific timing constraint under worst case conditions (i.e., establishing the feedback around the power converter to fix the output voltage), it is better to allow the voltage to vary such that the timing constraints are just met at any given temperature and operating conditions; this is accomplished by establishing the feedback around a

fixed processing rate or delay. Such embedded power supply systems can minimize energy consumption under varying temperature, process parameters, and computational workload. (Part III).

There is a wide range in power dissipation characteristics among the various circuit and logic styles (Part IV). Low-power circuit operation is achieved by reducing critical path delays and avoiding unnecessary transitions beyond what is required to implement the logic function. The ability to power down logic is important, and in some logic styles (e.g., self-timed circuits) this property is implicit. The design of energy recovery logic has gained significant interest, particularly in academia. Energy recovery logic reduces the energy dissipated per switching event by slowing down the transitions to such a level that there are negligible losses in the resistive components.

The scaling of technology into the submicron regime has forced interconnect to be an important factor of overall system power. As a result, it is necessary to develop architectures that minimize wirelengths by exploiting locality and decrease activity through coding techniques and reduced voltage swing (Part V). The voltage swing is decreased by exploiting on-chip regulators, charge sharing, and charge recycling techniques.

Embedded memory is an integral component of digital processors (Part VI). It is important to minimize unnecessary transitions (e.g., using hierarchical decoding schemes and self-timing) and voltage swing on heavily loaded bit-lines. Some techniques that minimize delay also minimize energy per access (e.g., low-swing). The scaling of supply voltages in memory circuits may require exploiting emerging technologies and circuit styles (like MTCMOS or self-reverse biasing techniques). Charge recycling techniques have also been shown to be effective in memory circuits.

By exploiting low-power techniques at all levels of the design, it is possible to reduce power dissipation by orders of magnitude. Several such systems are presented in Part VII, which includes examples of general purpose processors, programmable signal processors, and dedicated signal processors. Most of the gains come from aggressive scaling of supply voltages and avoiding unnecessary transitions (e.g., gated clock).

There has been significant activity in Computer-Aided Design tools for low-power systems. Two fundamentally different approaches for power estimation have been proposed which include probabilistic techniques (in which the node activities are computed in one pass through the logic) and statistical techniques (simulation based approaches). Effective solutions exist at all levels of the design abstraction ranging from logic and circuit to RTL, behavior software levels. Power optimization techniques, however, are not as mature at this point in time.

The second section in Part VIII give an indication of some of the optimization techniques being proposed and the types of power reductions that are presently possible using automated techniques.

It is believed that if the reader applies the appropriate techniques which have been presented here, they will also be able to achieve the orders of magnitude reduction in power consumption that has been shown to be possible. These dramatic results

have been obtained by designers for all classes of circuits which range from conventional microprocessors to highly-dedicated signal processing components. It is these kinds of results that indicate—through the era in which CMOS circuits can be designed without consideration for power consumption is gone—there is much that can be done so that the time for CMOS to be supplanted by yet another more energy efficient technology remains far in the future.

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