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WHY CMP?

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1.1 INTRODUCTION

Technology wonders have permeated into every facet of our daily life: fast computers with dual core processors and terabit hard drives, cell phones with cameras and GPS functions, video games with vivid graphics and superior sound, personal entertainment gadgets that go where we go, and smart implants that dose medicine on demand—just to name a few. These technology marvels that enable us to do things faster, more efficiently, and sometimes effortlessly all benefit from the advancements of semiconductor manufacturing processes. None of the advanced microelectronic devices could be built today without the continuous progress in shrinking the minimum feature size and increasing the circuitry complexity at the wafer level. The manufacturability of the smallest features or structures on a wafer is predominately determined or limited by the capability of the photolithographic step. To image lines or features accurately and precisely across the wafer, a photolithographic tool must be able to focus at all points of interest. For technology node dealing with relatively large features ($>0.5\ \mu\text{m}$), the photolithographic process with relatively high depth of focus can tolerate certain levels of topography on the surface. With the reduction in minimum feature size, the depth of focus is also sharply reduced. A minute surface topography or step height may lead to a loss in yield [1,2]. To overcome such a challenge, the microelectronic industry revitalized a set of polishing skills that have been serving mankind for generations and brought the craft to a state-of-the-art level to meet the challenges faced by the semiconductor industry. This rejuvenated process is now known as chemical–mechanical polishing or planarization (CMP). More

specifically, a CMP step was added in between each metallization and dielectric layer in wafer production to address the depth-of-focus issue in photolithography [3]. Soon the technique also enabled the implementation of copper as a better electric conductor, ending more than 40 years of monopoly of aluminum as an interconnect [4]. Since the publication of the first book dedicated to this topic in 1997 [5], the field has been flourished with innovations, discoveries, breakthroughs, and successful implementations. Part of this book will cover the new breakthroughs and discoveries with an emphasis on the chemistry behind the processes and the materials used in the applications. Furthermore, a focus will be placed on the correlation between the use of various consumables and their impact on the polishing outcome. The outlook of the technology will also be discussed in light of new applications and new solutions to persistent problems. This introductory chapter is organized according to the three major utilities of CMP—preparation of planar surfaces, formation of functional microstructures, and elimination of surface defects.

1.2 PREPARATION OF PLANAR SURFACE

1.2.1 Multilevel Metallization and the Need for Planarization

In a state-of-the-art integrated circuit, there are many active and passive elements including millions of transistors, capacitors, and resistors on a single chip [5]. In this ultra-large-scale integration (ULSI) era, the number of transistors per chip has already crossed the 40 million mark and is expected to increase to more than a billion over the next decade [6]. These discrete elements must be connected with conductive wiring to form a circuit. As chips become smaller and more complex, the demand for more efficient interconnect systems has also increased dramatically. One solution is to have multilevel wiring over the devices. A multilevel wiring scheme offers more direct routing and reduces the average length of connections among devices. This leads to a significant reduction in signal processing delays and improvement in chip performance (see Section 1.3.1 for details). Figure 1.1 shows a cross section of such a multilevel interconnect network in which metal lines are isolated by the dielectric and connected by vertical vias [5,7]. It is noted that the metal lines on the lower levels are much narrower in order to match the dimensions of the transistors and other microstructures. At top levels, the need for high-line density is reduced. Therefore, there are more rooms for wider lines. A wider line also helps to avoid the mismatch with the vertical vias. With the implementation of a multilevel metallization scheme, the packing density of the metal lines need not keep pace with the packing density at the gate level. Hence, interconnect dimensions need not shrink at the same pace as the gate-level dimensions [8]. This offers a potential for chip performance improvement without revamping the entire IC layout.

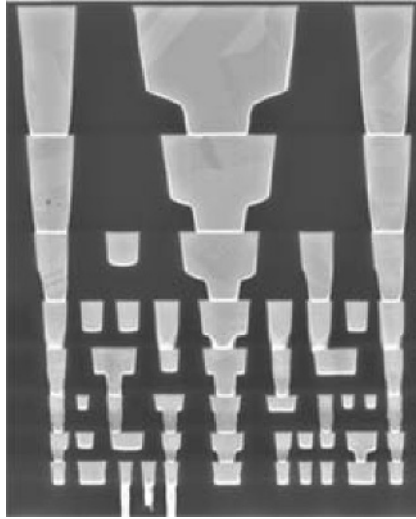


FIGURE 1.1 A cross section SEM image of a representative multilevel interconnect network (from Ref. 9).

The implementation of multilevel metallization presented immense opportunities for performance increase at the chip level. At the same time, the scheme also created enormous challenges in fabrication at the wafer level. The major source of such a challenge is the rugged topography buildup as the number of interconnect levels increases as shown in Fig. 1.2a [10]. The surface roughness has a direct negative impact on the accuracy and efficiency of pattern transfer onto photoresist with contact photolithography [11–19]. As the critical dimension of the device reduces, the depth of focus in photolithography also

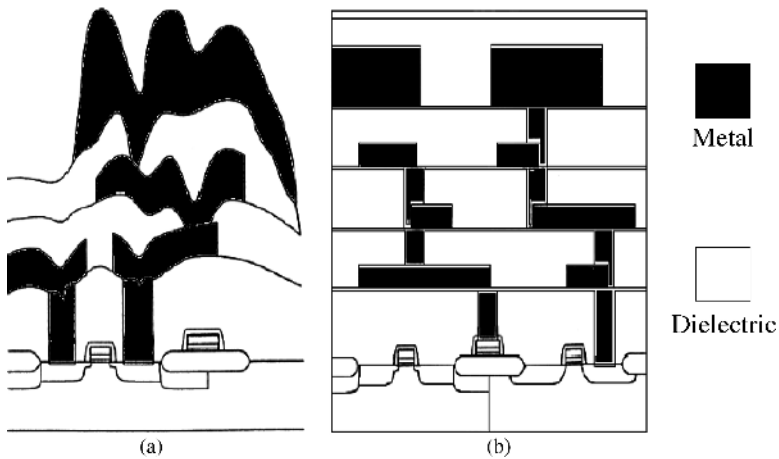


FIGURE 1.2 Devices fabricated without (left) and with (right) planarization (from Ref. 10).

diminishes. In other words, the topography or surface roughness will lead to a much wider distribution in focusing accuracy, which in turn translates to inaccurate patterning at significantly greater number of sites. For example, if the depth of focus for a particular feature size is in the order of $0.5\ \mu\text{m}$ determined by an optical lithography tool, any step heights larger than $0.5\ \mu\text{m}$ on the surface of pre- or intermetal dielectrics will cause improper patterning on the photoresist layer. Subsequently, the multilevel interconnect network will fail. The depth-of-focus limitation became insurmountable by any other techniques available at a fab when the critical dimensions dropped below $0.35\ \mu\text{m}$, which requires the surfaces to be planar within the same range. Driven by necessity, an effective planarization process was sought, envisioned, tested, and subsequently implemented. The process was CMP.

A comparison between a planarized and nonplanarized surface topography is shown in Fig. 1.2. By meeting the depth of focus requirement for the photolithographic step, CMP eliminated several yield-related issues such as missing contacts, undesired current leaks, and electromigrations [11–19].

1.2.2 Degrees of Planarization

The topography buildup on wafers is a combination of accumulated unevenness at feature, die, and wafer level. Other terms such as nanotopography, micro- or macrowaviness, and wharf have been used to describe such unevenness of a wafer at different length scales. To meet the requirement set by the depth of focus for subquarter micron technology, the roughness to be eliminated is in the regime of nanotopography and microwaviness. In other words, the step height of interest has an average wavelength of several microns to millimeters [1,5,20–23]. Similarly, depending on the net effectiveness on various types of topography, planarization processes can also be categorized as smoothing, local, and global planarizations. Some representative scenarios are illustrated in Fig. 1.3 [5,20–23].

As shown in Fig. 1.3, the least effective planarization is the so-called smoothing process that rounds off only the topography above the features. Local planarization generates a flat surface over an array of circuit features but does not significantly reduce topography at the edge of the array. To meet the requirement set by the depth of focus in the photolithography step, smoothing or local planarization is not adequate. A complete global planarization is desirable, but not required. A near-global planarization is often adequate. In other words, the planarization length is preferred in the order of 20–30 mm, which is the size of a typical die. As of today, there are no known processes that produce this effect over widely varying surface topographies and pattern layout densities other than CMP. CMP is the only technique that can produce planarization results that meet the requirements of lithography. The above discussion can be quantified by using a planarization length R (μm) and its corresponding angle θ (degrees) that are illustrated in Fig. 1.4.

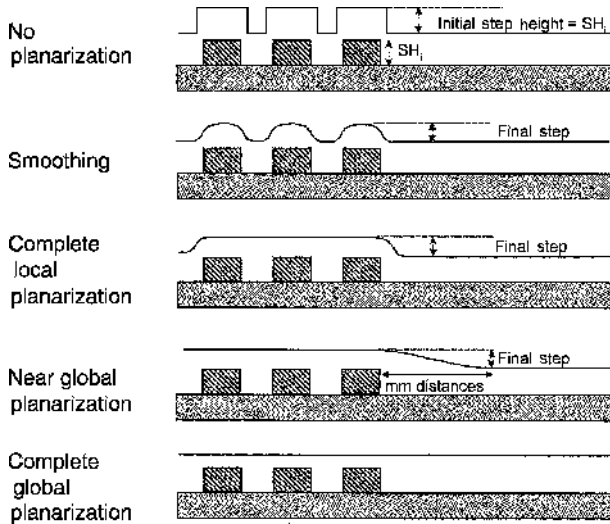


FIGURE 1.3 Levels of planarization that are relevant to semiconductor processing (from Ref. 5).

According to the definition given in Fig. 1.4, the following values of R and θ can be used to categorize degrees of planarization:

- Surface smoothing: $R = 0.1\text{--}2.0$ and $\theta > 30^\circ$.
- Local planarization: $R = 2.0\text{--}100$ and $30^\circ > \theta > 0.5^\circ$.
- Global planarization: $R \gg 100$ and $\theta < 0.5^\circ$.

1.2.3 Methods of Planarization

Several contending technologies are presently being used to achieve local and global planarizations that include spin on deposition (SOD), reflow of boron phosphorous silicate glass (BPSG), spin etch planarization (SEP), reactive ion etching and etch back (RIE EB), spin on deposition and etch back

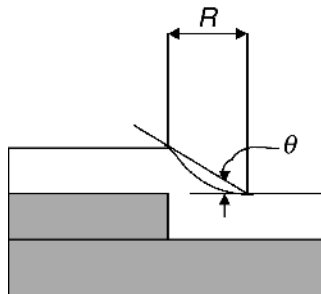


FIGURE 1.4 Planarization length R and slope θ (from Ref. 24).

(SOD + EB), and CMP. Among all these techniques, CMP is the only one that can offer excellent local and global planarities at the same time. More specifically, CMP can yield local planarization of features in the order of tens of microns and near-global planarization as far as tens of millimeters [5,20].

The modern-day CMP of dielectric materials for wafer processing has a root in glass polishing that has been practiced throughout civilization. The polishing mechanism has been widely studied and relatively well understood [5,20]. The process has also been vastly automated and perfected over the years. The substrates of glass polishing range from optical windows measured in submillimeters to telescope lenses that have diameters measured in meters. The consumables (pads and slurries) are essentially the same as those used in dielectric CMP. More specifically, other than some additional requirements, the silica- and ceria-based slurries used today for dielectric CMP bear resemblance to those used in glass polishing. Though more primitive in comparison to today's sophisticated polisher for CMP in a semiconductor fab, the glass polishing tool had the essential features even for the earliest applications. For example, Fig. 1.5 shows a picture illustrates the type of polisher used to polish the telescope lens in the Galileo era. In 1609, Galileo heard of the telescope while in Venice, and on his return, constructed one for himself. In 1610, Galileo published his telescopic discoveries in *The Starry Messenger* [25].

One who is well versed in CMP may choose to believe that the machine has the functions detailed below [26]. Can you identify them?

1. Variable speed platen.
2. Variable speed quill.

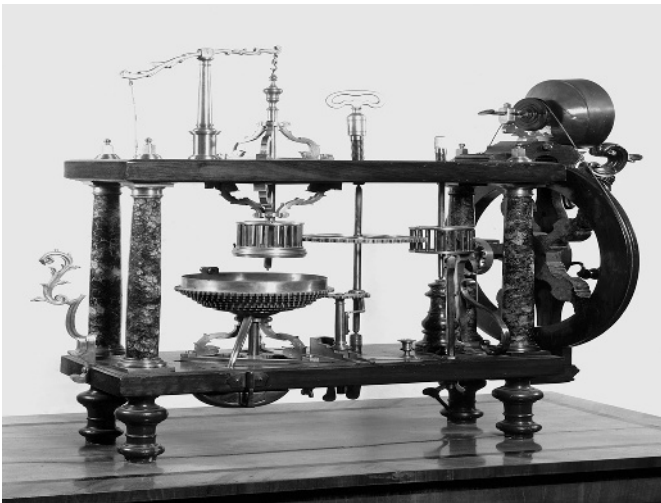


FIGURE 1.5 A highly ornamented Lens-grinding lathe on display at the Institute and Museum of the History of Science in Florence, Italy (from Ref. 26).

3. Vertical motion of the quill with variable downforce control.
4. Slurry dam and variable control of work piece slurry immersion.
5. Slurry drain.
6. Optional quill offset to provide eccentric polish head motion.

Prior to the implementation of CMP, various grinding and polishing techniques had been used in the semiconductor industry to planarize raw silicon wafers. In addition, to achieve a global flatness, the planarization process also removes the damage and defects caused by the sawing process to the single crystal. Because of the fact that silica and ceria do not chemically react with bare silicon, except the top oxidized silicon dioxide layer, the grinding and polishing process for this application is dominated by mechanical events.

1.2.4 Chemical and Mechanical Planarization of Dielectric Films

The most commonly implemented and extensively investigated CMP steps are the preparation of planar premetal dielectrics (PMD) and interlayer dielectrics (ILD) films on wafer. Together they are labeled as “oxide” CMP, as they both use the same materials that are based on silicon dioxide. Both processes share the integration concerns in deposition, planarity, and defectivity.

PMD CMP was designed to provide planarization between the front-end active devices and the back-end metallization. Several reasons for the planarization are (a) enabling contact lithography, (b) enabling contact etch uniformity, and (c) enabling contact tungsten CMP [5,20,21]. ILD CMP is meant to provide planarization between the increasing numbers of metal layers in the back end. The motivation is twofold: (a) enabling via lithography and (b) enabling via tungsten CMP. PMD and ILD CMP are “stop-in-film” processes [1,5,20,22–24,27,28]. There are no interfaces on which for CMP to stop. Therefore, the overall performance of the process is extremely dependent on consistent removal rate, within-die, within-wafer, and lot-to-lot uniformity.

In addition to the construction of a multilevel interconnect network, the semiconductor industry also improves the performance of IC chips by incorporating low-resistivity metal wiring such as copper and new dielectric materials with lower k constant (see Section 1.3.1 for details). The added benefit of using low- k dielectric materials includes a reduction in the crosstalk [29–31] and power dissipation [29–33]. The key challenge for the implementation of low- k materials is related to their intrinsic weak mechanical properties. Furthermore, in order to achieve a k value below 2.2, practically all materials are made with pores that exacerbate mechanical stability issue [29–33]. This is a particular concern for the CMP community as the operation invariably involves mechanical stress and shear force. In addition, practically all low- k dielectric materials are hydrophobic in nature. Upon exposure to moisture or wetness, the dielectric constant tends to increase. Therefore, unlike silicon-dioxide-based dielectric, the effective k constant may change after CMP. To

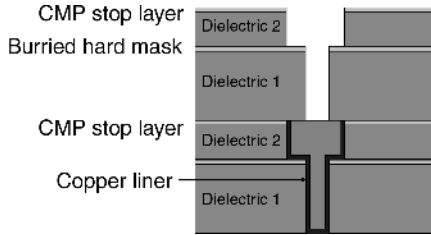


FIGURE 1.6 Incorporation of hard masks to protect the low- k dielectric materials (from Ref. 23).

overcome these challenges, an array of possible solutions has been explored and implemented. To mechanically protect the low- k dielectric material, a cap material sometimes is incorporated into the design of the device as shown in Fig. 1.6 [23]. Hard masks such as SiCN are incorporated to avoid the exposure of the low- k material to CMP consumables. This leads to the diversity of thin films that a CMP process will encounter. The hard masks also help to simplify lithography, etch, and clean.

1.2.5 Preparation of Planar Thin Films for Non-IC Applications Using CMP

Nearly every laptop or desktop computer in use today contains one or more hard disk drives. Every mainframe server and supercomputer is normally connected to hundreds of them. You can even find DVR, iPod, and camcorders that use hard disks instead of tape or flash memory. The computer hard drives store changing digital information on rigid magnetic memory disks. Figure 1.7 shows a stack of platters that have magnetic layers on them. Figure 1.8 shows a typical cross section of the rigid disk. In order to deposit the magnetic materials



FIGURE 1.7 A side view of a multiplaten computer hard drive (from Ref. 34).

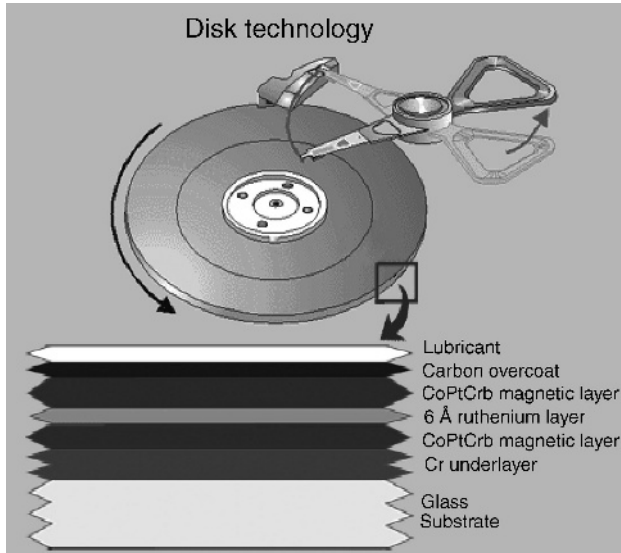


FIGURE 1.8 A cross section of a typical computer hard drive disk (from Ref. 35).

properly, the substrate must be perfectly flat and free of defects such as pits, scratch, and bumps. Any of these defects not only lower the effectiveness of the magnetic layer to store the information but also can cause the crash of read–write heads that are flying over the platen at a tremendous speed and impressive low altitude. The operation can be compared to a situation where a large aircraft is flying at the top speed, less than a meter above the ground. Any nanoasperity on the computer hard drive disk is equivalent to an insurmountable mountain for the aircraft to avoid. Therefore, a CMP process has been used to planarize the substrates for the computer hard drives. There are two major types of substrates used in today’s computer hard drives. One is glass based: ceria (CeO_2) particles are the most commonly used abrasive for this application. The other is aluminum coated with NiP. The NiP layer is usually electrochemically plated and then subsequently planarized with alumina-based slurry followed by silica-based slurry to remove the defects and nanoasperities. The surface roughness after the CMP process is often required to be less than 1 Å.

1.3 FORMATION OF FUNCTIONAL MICROSTRUCTURES

1.3.1 RC Delay and New Interconnect Materials

Miniaturization of semiconductor devices has been a continuous trend in the microelectronics industry. The decrease in minimum feature length reduces the overall device size, increases the packing density, and thus reduces the cost of

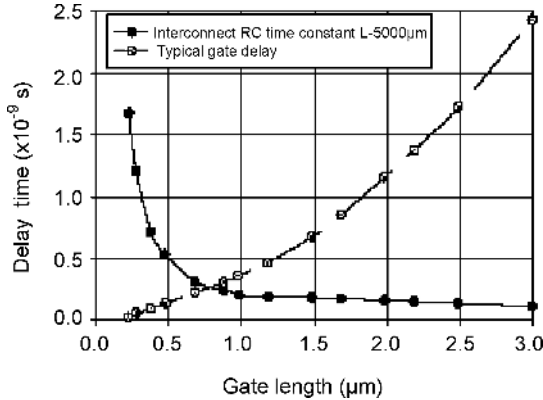


FIGURE 1.9 Delay time vs. gate length (from Ref. 41).

function [5,37,38]. In the past 50 years, prices per transistor have gone down 100 million times. The minimum size of devices such as transistors has been reduced by a factor of a billion [19,39]. However, as the feature size scales down to below $0.5 \mu\text{m}$, the improvement of device performance such as speed is hindered by the delays in signal processing. In a typical device, there are two major sources of processing delays—intrinsic gate delay and interconnect delay [36]. The intrinsic gate delay is the time required to switch the transistor on or off [40]. Interconnects are the metal wires that connect different devices on a chip among themselves and the outside world [20]. The interconnect delay is the time spent for a signal to propagate from the source to its destination in a circuit. The total delay in signal processing is the sum of interconnect delay and the device delay. As shown in Fig. 1.9, the gate delays typically decrease as the gate length decreases. The interconnect delays on the contrary increase as the gate length decreases. As the device sizes reduce below the sub-micron level (below $0.5 \mu\text{m}$), the total delay is dominated by the interconnect delay.

The two key components in interconnect delays include the inherent resistance (R) of the metal lines and the capacitance (C) of the dielectric material in between the lines. The so-called RC delay is defined as the time required for the voltage at one end of a metal line to reach 63 % of its final value when a step input is presented at the other end of the line [18]:

$$RC = \rho \epsilon l^2 / td \quad (1.1)$$

where R is the resistance of the interconnect, C is the capacitance of the dielectric in between the lines, ρ is the resistivity of the interconnect, ϵ is the permittivity of the insulator, t is the thickness of the insulator, and d is the thickness of the metal line or interconnect.

There are two types of capacitances associated with interconnect—the line-to-ground capacitance and line-to-line capacitance as illustrated in Fig. 1.10. Although line-to-substrate capacitance decreases as the feature size decreases,

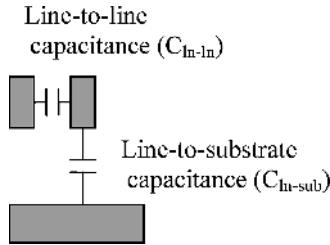


FIGURE 1.10 Two categories of capacitance (from Ref. 41).

the line-to-line capacitance (or the interconnect delay) increases with the reduction of the feature size. To reduce the total delay in signal processing along with the chip miniaturization, the industry took a parallel approach—replacing the traditional interconnect material (Al) with a better conductor (Cu) and substituting traditional silicon dioxide with low-*k* dielectric materials.

The first generation of the interconnect material is aluminum with a resistivity of $\rho = 2.66 \mu\Omega \text{ cm}$. One approach to reduce *RC* delay is to switch to an interconnect material with lower resistivity as indicated by Eq. (1.1). A wide range of metals was considered as a potential candidate in the early 1990s. Gold has excellent resistance to corrosion and electromigration but its conductivity is similar to that of aluminum. Silver has the lowest resistivity ($\rho = 1.59 \mu\Omega \text{ cm}$) but poor resistance to corrosion and electromigration. Hence, copper that has a resistivity of $1.67 \mu\Omega \text{ cm}$ and excellent resistance to electromigration was selected. Compared to aluminum, copper has one drawback. It cannot be deposited by RIE. Therefore, a copper interconnect is typically formed via a damascene process in which a pattern is first etched into the dielectric and overfilled with copper. The excess copper above the

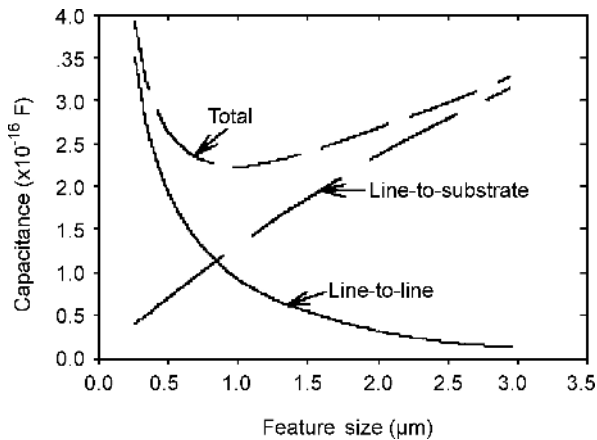


FIGURE 1.11 Capacitance vs. feature size (from Ref. 41).

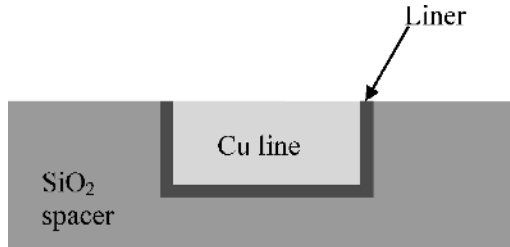


FIGURE 1.12 Typical layout of a trench showing Cu, dielectric, and barrier (Ta or TaN) (from Ref. 42).

trench is then removed. The copper remaining in the trench forms individual lines (Fig. 1.12). Copper has poor adhesion to dielectric materials such as silicon dioxide. Compared to aluminum, copper is also more liable to diffuse into SiO_2 . To address the adhesion and diffusion issues, a barrier is placed between the copper and the dielectric [1,42]. There are several possible candidates for barrier materials, a combination of Ta and TaN has been the choice for many successful manufacturing processes.

1.3.2 Damascene and Dual Damascene [11]

Damascene “Damasquinado de Oro” or “Damasquino” is an art of decorating nonprecious metals with gold. It has roots in the Middle Ages and originates from the oriental-style artisan work done in Damascus, Syria. The craft, perfected by the Arabs and brought with them to Spain, has remained virtually unchanged over the centuries. Figure 1.13 shows a piece of jewelry made with a damascene process.



FIGURE 1.13 A typical piece of jewelry made with a damascene process (from Ref. 43).

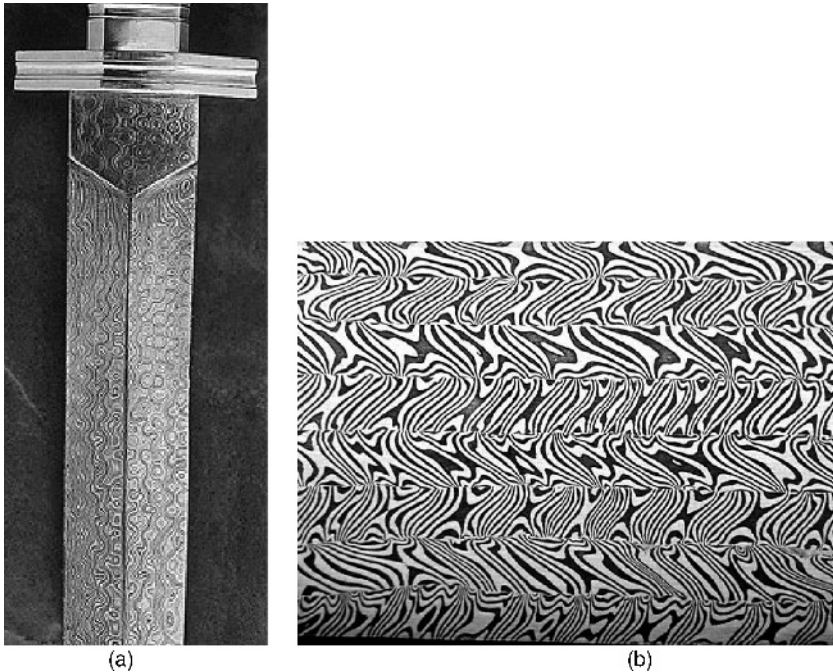


FIGURE 1.14 Sword made with a damascene process (a) and typical patterns on a damascus metal (b) (from Ref. 44,43).

The technique was apparently also used to make the legendary Damascus swords. The details for making Damascus steel remain a mystery even with the presence of numerous well-preserved samples. Recent research into the structure and composition of the steel reveals that the strength of the steel was a result of carbon nanotubes and carbide nanowires present in the structure of the forged metal. Damascus swords often had an obvious patterned texture on their surfaces (Fig. 1.14).

The semiconductor industry borrowed the word damascene to describe the patterned metal line formation process. Figure 1.15 illustrates a basic process for the formation of a copper line via a damascene process. The advantage of using copper is that it could be used as both an interconnect and a via; hence, the method of dual damascene comes into play. This method has come into use after the introduction of copper. In short, it can be said as opposite to that of RIE used for patterning aluminum. The oxide is etched to form patterns required for patterns of wires or vias. The barrier is then deposited followed by copper. The excess burden of copper is removed by using CMP, believed to be the only technique that gives global planarization. The process eliminates the etching of copper and maintains planar surfaces necessary for multilevel metallization. The process of dual damascene eliminates complexity by reducing the number of steps in the patterning process. It also reduces the

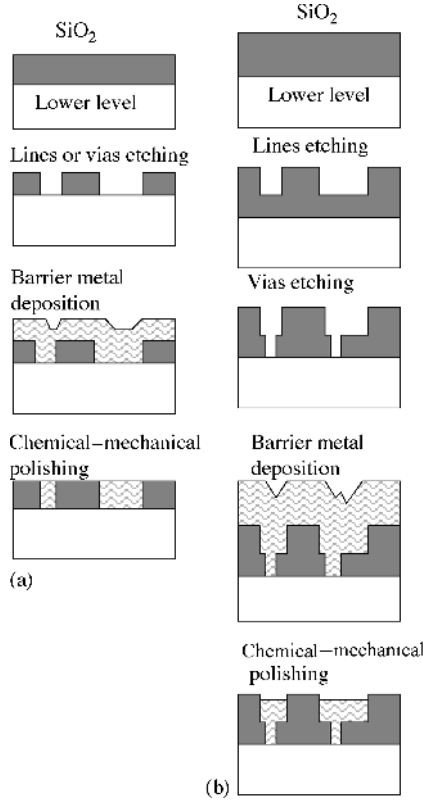


FIGURE 1.15 Damascene and dual damascene techniques employed (from Ref. 45).

risk of failure between metal and via. The schematics of both single and dual damascene are shown in Fig. 1.15.

The low-resistivity and high-electromigration properties have made copper the material of choice for the fabrication of interconnects in present-day IC

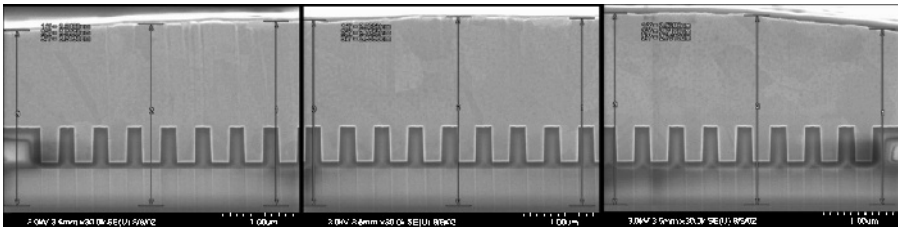


FIGURE 1.16 Cross section SEM image of copper wafer showing overburden Cu with underlying features. The features shown are 50% in metal:dielectric density and 2 μm in width (from Ref. 46).

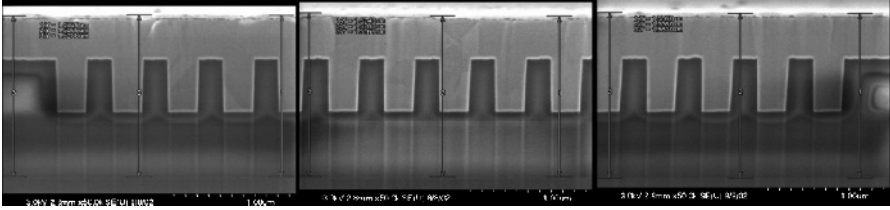


FIGURE 1.17 Cross section SEM image of copper wafer after the removal of the overburden with the achievement of planarization. The features shown are 50% in density and $2\ \mu\text{m}$ in width (from Ref. 46).

chips. The inability of copper to form volatile compounds at lower pressures to assist RIE has left damascene as the only viable process to incorporate copper through CMP. Because of the copper migration issue, the interconnect lines are not directly in contact with the dielectric. A diffusion barrier is required to protect the integrity of the line. Therefore, after the removal of overburden copper, the barrier is also removed. A typical multistep Cu CMP process involves three steps: the overburden copper is initially planarized, which is followed by a Cu-clearing step. The third step involves the clearing of the barrier metal. Figure 1.16–1.19 clearly illustrate the three steps described [46]. Figures 1.20 and 1.21 show a closer view of typical features before and after the barrier CMP.

After the removal of the copper barrier layer (usually made of Ta and TaN), the feature needs to be perfectly flat between the three materials (dielectric, barrier, and copper line). A representative SEM image of such a result is shown in Fig. 1.22.

1.3.3 Tungsten CMP

The main application of tungsten CMP is to create the so-called tungsten plugs that provide the vertical links between in-line wiring. As shown in Fig. 1.1, the number of such plugs decreases as the size of such plugs increases at higher metallization level. Figure 1.22 shows a representative tungsten plug [48]. It is

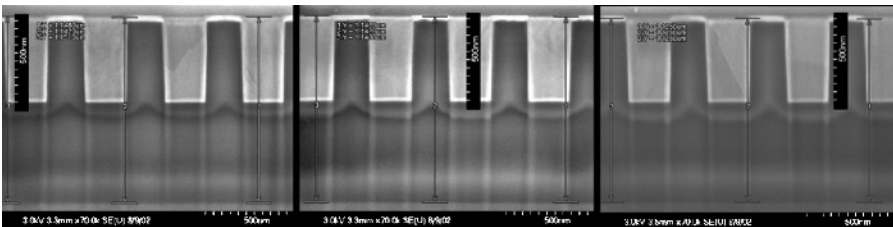


FIGURE 1.18 Cross section SEM image of copper wafer after copper clearing step. The barrier is still present at this stage. The features shown are 50% in density and $2\ \mu\text{m}$ in width (from Ref. 46).

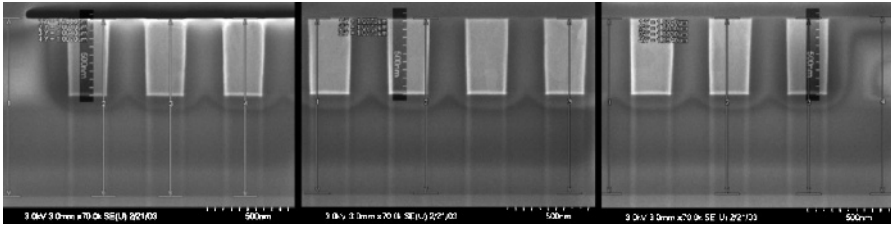


FIGURE 1.19 Cross section SEM image of copper wafer after the removal of barrier (from Ref. 46).

noted that it will take three damascene processes to create such a structure: first construction of a copper line, then a tungsten plug, and then another copper line [49]. Similar to copper CMP, tungsten plug also requires an adhesion and diffusion layer (Ti and TiN) [1,50]. Therefore, a W CMP process is actually a combination of tungsten, titanium, and titanium nitride removal, all in one step.

1.3.4 STI

Another important microstructure in IC manufacturing process is shallow trench isolation (STI) that allows the effective separation of active devices and increase of packing densities. Figure 1.23 shows a schematic of an STI structure before and after polishing [51]. It is important for the dishing of the oxide in the trench and the nitride loss to be as low as possible.

With the various types of CMP described above (dielectric and metal CMP), a multilevel interconnect network can be constructed. Impressive progress

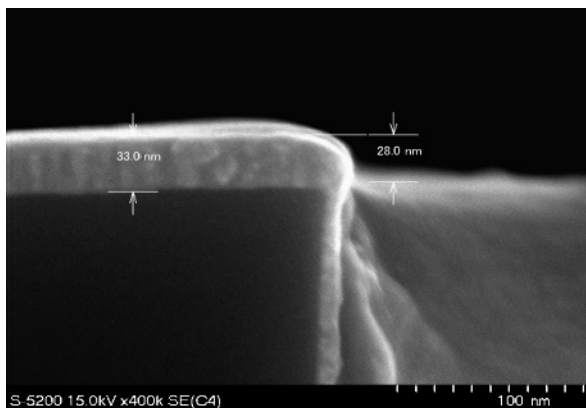


FIGURE 1.20 Cross section SEM image of a copper interconnect after the removal of overburden copper and before the removal of barrier layer (from Ref. 47).

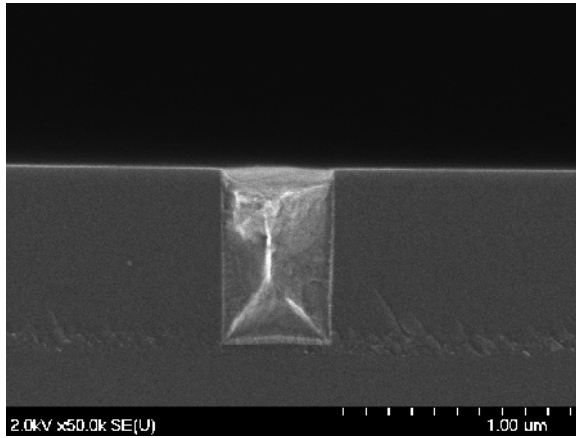


FIGURE 1.21 Cross section SEM image of a copper interconnect after the removal of overburden copper and barrier layer (from Ref. 47).

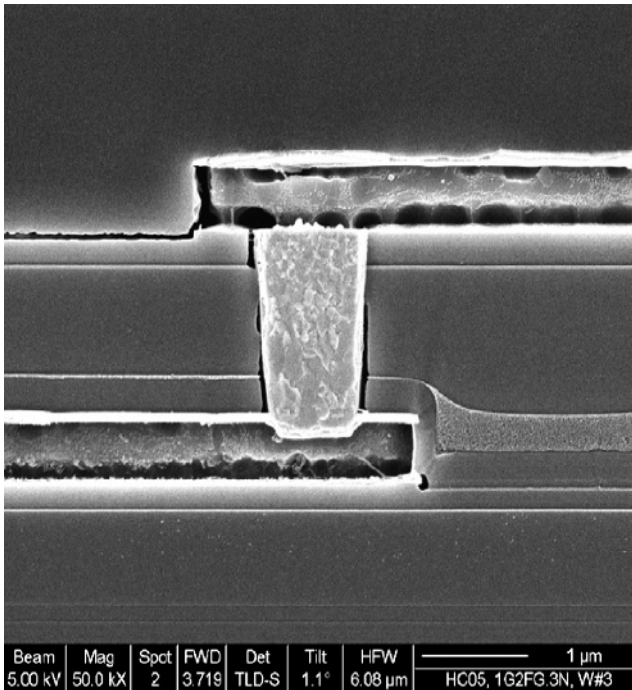


FIGURE 1.22 Cross section SEM image of a representative tungsten plug in between two copper lines (from Ref. 48).

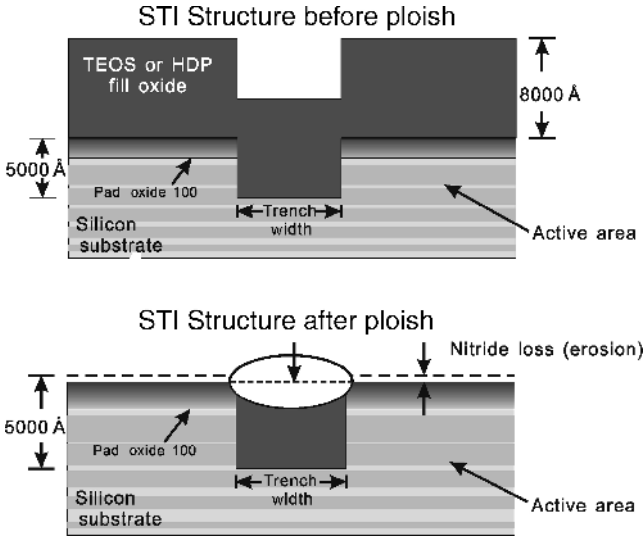


FIGURE 1.23 Schematic of an STI structure before and after polishing (from Ref. 51).

has been made over the past decade in constructing such a complex and dense network that provides the much needed boost to the IC performance. Fig. 1.24 shows the sharp contrast of the level of complexity in IC chip manicuring. Figure 1.24a shows the very first IC with four transistors on a single level of metal connection. Figure 1.24b shows, 37 years later, over 40 millions of transistors packed into a single IC with multilevel interconnects [6].

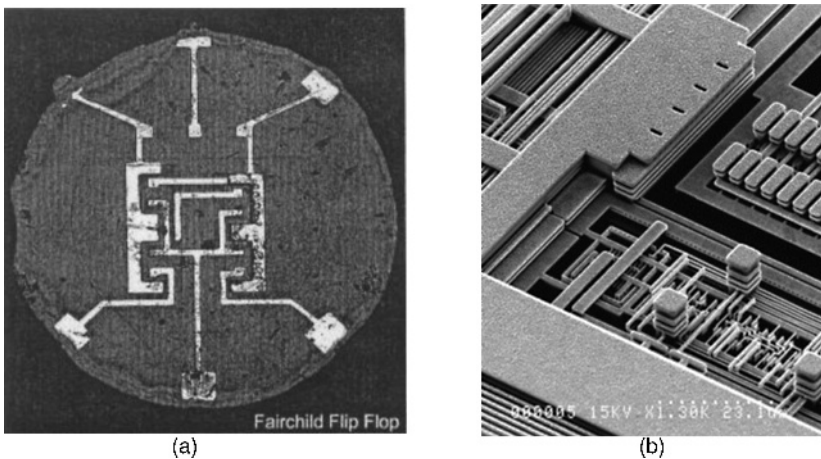


FIGURE 1.24 The first IC built on single layer of metal connect that links four transistors (a) and the IC with multilevel interconnect (b) (from Ref. 52).

1.4 CMP TO CORRECT DEFECTS

The application of CMP could also be extended to the reduction of surface defects in addition to the preparation of planar surfaces and fabrication of functional microstructures. As matter of fact, these types of applications have already been implemented in some cases as a part of the planarization process. For example, at the end of a copper or tungsten CMP process, a buffing step is inserted to remove residues, particles, and correct some minor defects such as shallow scratches. The buffing process is typically carried out on the last platen using DI water or a solution that is similar to those used in a post-CMP cleaning. In most cases, a buffing procedure is performed on a much softer pad [53,54]. Sometimes, owing to tool limitation or other concerns, the same pad or platen is used. Chen and co-workers [53] employed a buffing process on the same pad employed for polishing to reduce the residue silica abrasives. The silica abrasives were believed to be chemisorbed onto the copper oxide surface. Instead of DI water, a solution of HNO_3/BTA was used in this buffing process. The presence of nitric acid helped to etch a thin layer of copper oxide and loosen the particle adhesion to the surface. The presence of BTA as a passivating agent protects the copper surface from excessive etching or corrosion. The wafers were subsequently scrubbed to eliminate the residual particles. Cheemalapati et al. demonstrated the usefulness of an in situ buffing step to reduce the organic residue left by a copper CMP process. More specifically, at the near end of a copper clearing process, the copper slurry was substituted with a post-CMP cleaning solution for a short period of time. The extent of the organic residue was significantly reduced. This is particularly useful if the organic residue becomes difficult to clean after the wafer is exposed to air [55]. The elimination of preexisting scratches using a CMP step on copper blanket wafers was also shown by Hegde and Babu [56]. Different copper CMP slurries with and without the abrasives were studied for the effectiveness of removing the preexisting scratches. The ratio between the removal rate and the static etch rate was found to be the dominating factor in determining the depth of scratch that could possibly be removed. The application of such processes could possibly become useful for a three-step Cu CMP process that employs multiple slurries.

For some applications, the crystalline structure of a surface has a significant impact on the proper growth of the next layer of materials. The surface not only must be perfectly planar but also must be free from crystal lattice defects. For example, sapphire is a widely used material for blue emitting diode, laser diode devices, visible–infrared window, and random applications. Although there is a large mismatch in the lattice constants and thermal expansion coefficient between nitride and sapphire, sapphire is still known as the most commonly used substrate in the GaN device for its physical robustness and high-temperature stability. The performance of these devices is highly dependent on the quality of the substrate surface processing. Wang et al.

TABLE 1.1 Advantages of CMP.

Benefits	Remarks
Planarization	Achieves global planarization
Planarize various materials	Wide range of wafer surfaces can be planarized
Planarize multimaterial surfaces	Useful for planarizing multiple materials during the same polish step
Reduce severe topography	Reduces severe topography to allow fabrication with tighter design rules an additional interconnection levels
Alternative method of metal patterning	Provides an alternative means of patterning metal, eliminating the need to plasma etch, difficult to etch metals and alloys
Improved metal step coverage	Improves metal step coverage due to reduction in topography
Increased IC reliability	Contributes to increasing IC reliability, speed, yield (lower defect density) of sub-0.5 μm circuits
Reduce defects	CMP is a subtractive process and can remove surface defects
No hazardous gases	Does not use hazardous gas common in dry etch process

demonstrated that CMP followed by a chemical etching yields the best quality sapphire substrate surfaces [57–60].

1.5 ADVANTAGES AND DISADVANTAGES OF CMP

A list of advantages and disadvantages of CMP are shown in Tables 1.1 and 1.2, respectively [15]. By no means are the lists complete, but they offer some useful comparisons with other associated or competing technologies.

TABLE 1.2 Disadvantages of CMP.

Disadvantages of CMP	Remarks
New technology	CMP is a new technology for wafer planarization. There is relatively poor control over process variables with narrow process latitude
New defects	New types of defects from CMP can affect die yield. These defects become more critical for sub-0.25 μm feature sizes
Need for additional process development	CMP requires additional process development for process control and metrology. An example is the endpoint of CMP is difficult to control for desired thickness
Cost of ownership is high	CMP processes materials require high maintenance and frequent replacements of chemicals and parts

1.6 CONCLUSION

CMP emerged as an enabling technique for the semiconductor industry to overcome the depth-of-focus challenge for the implementation of a multilevel interconnect scheme. Soon, the technique was adapted to assist the formation of STI microstructures and vertical tungsten via. The introduction of copper as a new interconnect material helped launch CMP as an independent field with broad participation of scientists and engineers from a wide range of disciplines including chemistry, physics, materials science, and chemical and mechanical engineering. The number of patents, publications, and conferences dedicated to CMP processes has dramatically increased over the past 15 years. From an application point of view, CMP is able to not only prepare planar surfaces with impressive planarization length but also enable the formation of microstructures such as copper lines, tungsten vias, and STI. The process can be so well controlled that the technique could also be implemented to remove surface defects from prior manufacturing steps. From the operations point of view, the industry has built an infrastructure consisting of polishers, metrology tools, slurry delivery, consumable management, and matching supply chains. The cost of tool ownership is declining. This will help the implementation of this process in the fab for both routine techniques and new applications.

QUESTIONS

1. Fundamentally, other than the three major types of applications of CMP described in this chapter, what other types of application also exist or can be developed?
2. Why is the planarization length desirable at die size? Will a planarization length at wafer diameter scale really be an advantage?
3. Other than the damascene process, is there any other way to form microstructures such as copper lines, tungsten vias, and STI?
4. In addition to Tables 1.1 and 1.2, what are the other potential advantages and disadvantages of CMP in relationship to competing technologies?

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