

Preface

Phase-locked loops (PLLs) and clock recovery circuits (CRCs) find wide application in wireless and communication systems, disk drive electronics, high-speed digital circuits, and instrumentation. While the theory of operation of these circuits has long been developed and treated in a number of books (including two reprint collections published by IEEE Press in the 1970s and 1980s), design techniques for monolithic implementation of PLLs and CRCs in modern integrated-circuit (IC) technologies have appeared only recently, primarily in the form of conference and journal papers. For an IC designer entering this field, theoretical books often have too many details and IC-related publications too few.

This book deals with the analysis, design, simulation, and implementation of PLLs and CRCs in monolithic technologies. It has been organized with two goals in mind: first, to bridge the existing gap between the theory and the design of phase-locked systems, and second, to selectively present the published work on PLLs and CRCs in a coherent, unified volume, providing a self-contained reference for students and practicing engineers.

In studying phase-locked loops (PLLs), one encounters two difficulties. First, the basic PLL is deceptively simple, often tempting the reader to ignore the crucial details that determine the performance in a realistic environment. Second, the design of PLLs cannot be easily described using a straight “top-down” or “bottom-up” approach, because each level of abstraction entails issues strongly related to other levels as well.

In order to overcome the above difficulties, this book begins with a tutorial on phase-locked loops and clock recovery circuits. The goal is to develop an intuitive understanding of the underlying principles and describe the important issues, preparing the reader for more advanced topics in the following collection of papers. The tutorial itself is organized in a “bottom-up–top-down” sequence to gradually take the reader from basic components to the architecture level and back to the building blocks.

Following the tutorial are the selected papers, organized in five parts. Part I deals with theoretical aspects of PLLs, covering topics such as transient and frequency response, discrete-time analysis, frequency detection, and phase noise.

Part II is concerned with the design of PLL and CRC building blocks, in particular oscillators and phase/frequency detectors for both periodic and random binary waveforms.

Part III addresses the difficult issue of PLL modeling and simulation. SPICE macromodeling, nonlinear mathematical modeling, and high-level behavioral representation are described.

Parts IV and V present papers on monolithic implementation of PLLs and CRCs, respectively, demonstrating a wide range of speeds for various applications, from fiber optics to microprocessors.

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