

# Contents

<b>Preface</b>	<b>xi</b>
<b>Part I Introduction and Tutorial</b>	<b>1</b>
Synthesis Techniques	
V. F. Kroupa	<b>3</b>
<b>Part II Direct Digital Single-Frequency Synthesizers</b>	<b>17</b>
A Frequency Synthesizer for $10/2\pi$ kHz	
G. W. Small ( <i>IEEE Transactions on Instrumentation and Measurement</i> , March 1973).	<b>19</b>
Approximating Frequency Synthesizers	
V. F. Kroupa ( <i>IEEE Transactions on Instrumentation and Measurement</i> , December 1974).	<b>23</b>
<b>Part III Wide-Range Direct Digital Frequency Synthesizers</b>	<b>27</b>
A Digital Frequency Synthesizer	
J. Tierney, C. M. Radre, and B. Gold ( <i>IEEE Transactions on Audio and Electroacoustics</i> , March 1971).	<b>29</b>
CMOS/SOS Frequency Synthesizer LSI Circuit for Spread Spectrum Communications	
D. A. Sunderland, R. A. Strauch, S. S. Wharfield, H. T. Peterson, and C. R. Cole ( <i>IEEE Journal of Solid-State Circuits</i> , August 1984).	<b>38</b>
A High-Speed Direct Frequency Synthesizer	
P. H. Saul and D. G. Taylor ( <i>IEEE Journal of Solid-State Circuits</i> , February 1990).	<b>47</b>
Single Chip 500 MHz Function Generator	
P. H. Saul, W. Barber, D. G. Taylor, and T. Ward ( <i>IEE Proceedings-G</i> , April 1991).	<b>52</b>
Low-Latency, High-Speed Numerically Controlled Oscillator Using Progression-of-States Technique	
M. Thompson ( <i>IEEE Journal of Solid-State Circuits</i> , January 1992).	<b>57</b>
<b>Part IV Spurious Signals in Direct Digital Frequency Synthesizers</b>	<b>63</b>
Spectra of Pulse Rate Frequency Synthesizers	
V. F. Kroupa ( <i>Proceedings of the IEEE</i> , December 1979).	<b>65</b>
Noise Spectra of Digital Sine-Generators Using the Table-Lookup Method	
S. Mehrgardt ( <i>IEEE Transactions on Acoustics, Speech, and Signal Processing</i> , August 1983).	<b>68</b>
An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation	
H. T. Nicholas III, and H. Samueli ( <i>Proceedings of the 41st Annual Frequency Control Symposium</i> , 1987).	<b>71</b>
The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects	
H. T. Nicholas III, H. Samueli, and B. Kim ( <i>Proceedings of the 42nd Annual Frequency Control Symposium</i> , 1988).	<b>79</b>
Methods of Mapping From Phase to Sine Amplitude in Direct Digital Synthesis	
J. Vankka ( <i>IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control</i> , March 1997).	<b>86</b>
A 150-MHz Direct Digital Frequency Synthesizer in 1.25- $\mu\text{m}$ CMOS with $-90$ -dBc Spurious Performance	
H. T. Nicholas III, and H. Samueli ( <i>IEEE Journal of Solid-State Circuits</i> , December 1991).	<b>95</b>

An Exact Spectral Analysis of a Number Controlled Oscillator Based Synthesizer J. F. Garvey and D. Babitch ( <i>Proceedings of the 44th Annual Frequency Control Symposium</i> , 1990).	106
<b>Part V      Reduction of Spurious Signals in Direct Digital Frequency Synthesizers</b>	<b>117</b>
Spurious Suppression in Direct Digital Synthesizers C. E. Wheatley and D. E. Phillips ( <i>Proceedings of the 35th Annual Frequency Control Symposium</i> , 1981).	119
A Low-Frequency, High Resolution Digital Synthesizer R. P. Giffard and L. S. Cutler ( <i>Proceedings—IEEE International Frequency Control Symposium</i> , 1997).	127
A Spurious Reduction Technique for High-Speed Direct Digital Synthesizers L. J. Kushner and M. T. Ainsworth ( <i>Proceedings of the IEEE International Frequency Control Symposium</i> , 1996).	132
A Direct-Digital Synthesizer with Improved Spectral Performance P. O’Leary and F. Maloberti ( <i>IEEE Transactions on Communications</i> , July 1991).	140
Spur-Reduced Digital Sinusoid Synthesis M. J. Flanagan and G. A. Zimmerman ( <i>IEEE Transactions on Communications</i> , July 1995).	143
Spectral Properties of DDFS: Computer Simulations and Experimental Verifications V. F. Kroupa (Adaptation: <i>1993 and 1994 IEEE International Frequency Control Symposia and the 8th European Frequency and Time Forum</i> , March 1994).	152
<b>Part VI      Combination of DDFS with Phase Locked Loops (PLLs)</b>	<b>165</b>
Principles of Phase Locked Loops (PLL) V. F. Kroupa (A specially written paper for this volume).	167
Low-Noise Microwave-Frequency Synthesizers: Design Principles V. F. Kroupa ( <i>IEE Proceeding-H</i> , December 1983).	175
A J-Band Spread-Spectrum Synthesizer Using a Combination of DDS and Phaselock Techniques M. V. Harris ( <i>Colloquium on “Direct Digital Frequency Synthesis,” IEEE Digest No: 1991/172</i> , November 1991).	181
Principles of Fractional-N Frequency Synthesizers V. F. Kroupa (A specially written paper for this volume).	191
A Multiple Modulator Fractional Divider B. Miller and R. J. Conley ( <i>IEEE Transactions on Instrumentation and Measurements</i> ). June 1991.	197
A Fast-Settling GaAs-Enhanced Frequency Synthesizer J. F. Naber, H. P. Singh, W. J. Tanis, A. J. Koshar, and G. L. Segalla ( <i>IEEE Journal of Solid-State Circuits</i> , October 1992).	203
<b>Part VII      Phase and Background Noise in DDFS</b>	<b>207</b>
Introduction to the Noise Properties of Frequency Sources V. F. Kroupa (A specially written paper for this volume).	208
Close-to-the-Carrier Noise in DDFS V. F. Kroupa ( <i>Based on a paper that originally appeared in the IEEE International Frequency Control Symposium</i> , November 1996).	216
Phase Noise in Direct Digital Synthesizers E. M. Mattison and L. M. Coyle ( <i>Proceedings of the 42nd Annual Frequency Control Symposium</i> , 1988).	224
A Direct Digital Synthesizer with 100-MHz Output Capability P. H. Saul and M. S. J. Mudd ( <i>IEEE Journal of Solid-State Circuits</i> , June 1988).	229
An Analysis Methodology to Identify Dominant Noise Sources in D/A and A/D Converters J. A. Connelly and K. P. Taylor ( <i>IEEE Transactions on Circuits and Systems</i> , October 1991).	232

<b>Part VIII</b>	<b>Digital-to-Analog Converters</b>	<b>245</b>
Digital-to-Analog Converters		
	V. F. Kroupa (A specially written paper for this volume).	<b>246</b>
A Monolithic 10-b Digital-to-Analog Converter Using Ion Implantation		
	G. Kelson, H. H. Stellrecht, and D. S. Perloff ( <i>IEEE Journal of Solid-State Circuits</i> , December 1973).	<b>257</b>
An Inherently Monotonic 12 Bit DAC		
	J. A. Schoeff ( <i>IEEE Journal of Solid-State Circuits</i> , December 1979).	<b>265</b>
An 8-Bit, 5 ns Monolithic D/A Converter Subsystem		
	P. H. Saul, P. J. Ward, and A. J. Fryers ( <i>IEEE Journal of Solid-State Circuits</i> , December 1980).	<b>273</b>
A 500-MHz 8-Bit D/A Converter		
	K. Maio, S.-I. Hayashi, M. Hotta, T. Watanabe, W. Ueda, and N. Yokozawa ( <i>IEEE Journal of Solid-State Circuits</i> , December 1985).	<b>280</b>
An 8-Bit 2-ns Monolithic DAC		
	T. Kamoto, Y. Akazawa, and M. Shinagawa ( <i>IEEE Journal of Solid-State Circuits</i> , February 1988).	<b>284</b>
<b>Part IX</b>	<b>State of the Art and Some Applications</b>	<b>289</b>
A High Purity, High Speed Direct Digital Synthesizer		
	G. W. Kent and N.H. Sheng ( <i>Proceedings of the IEEE International Frequency Control Symposium</i> , 1993).	<b>291</b>
A 200 MHz Quadrature Digital Synthesizer/Mixer in 0.8 $\mu\text{m}$ CMOS		
	L. K. Tan and H. Samuelli ( <i>IEEE Journal of Solid-State Circuits</i> , March 1995).	<b>296</b>
An 800-MHz Quadrature Digital Synthesizer with ECL-Compatible Output Drivers in 0.8 $\mu\text{m}$ CMOS		
	L. K. Tan, E. W. Roth, G. E. Yee, and H. Samuelli ( <i>IEEE Journal of Solid-State Circuits</i> , December 1995).	<b>304</b>
A Dual Frequency Synthesis Scheme for a High C-Field Cesium Resonator		
	E. Rubiola, A. Del Casale, A. De Marchi, ( <i>Proceedings of the IEEE International Frequency Control Symposium</i> , 1993).	<b>314</b>
<b>Part X</b>	<b>New Ideas for the DDFS Design</b>	<b>319</b>
A 700-MHz 24-b Pipelined Accumulator in 1.2- $\mu\text{m}$ CMOS for Applications as a Numerically Controlled Oscillator		
	F. Lu, H. Samuelli, J. Yuan, and H. Svensson ( <i>IEEE Journal of Solid-State Circuits</i> , August 1993).	<b>320</b>
An Integrated GaAs 1.25 GHz Clock Frequency FM-CW Direct Digital Synthesizer		
	N. Caglio, J.-L. Degouy, D. Meignant, P. Rousseau, and B. Leroux ( <i>IEEE GaAs Symposium</i> , October 1993).	<b>328</b>
The Composite DDS—A New Direct Digital Synthesizer Architecture		
	L. J. Kushner ( <i>Proceedings of the IEEE International Frequency Control Symposium</i> , 1993).	<b>332</b>
A Narrow Band High-Resolution Synthesizer Using a Direct Digital Synthesizer Followed by Repeated Dividing and Mixing		
	R. Karlquist ( <i>Proceedings of the IEEE International Frequency Control Symposium</i> , 1995).	<b>338</b>
A 3 to 30 MHz High-Resolution Synthesizer Consisting of a DDS, Divide-and-Mix Modules, and a M/N Synthesizer		
	R. Karlquist ( <i>Proceedings of the IEEE International Frequency Control Symposium</i> , 1996).	<b>347</b>
A New Architecture for a Sinewave Output DDS With a High Spectral Purity		
	L. Lo Presti, G. Cardamone, A. De Marchi, and E. Rubiola ( <i>8th European Frequency and Time Forum</i> , March 1994).	<b>352</b>
<b>Part XI</b>	<b>Mathematical Background</b>	<b>359</b>
Quasiperiodic Omission of Pulses		
	V. F. Kroupa (A specially written paper for this volume).	<b>360</b>
Useful Computer Programs for Investigations of Spurious Signals in DDFS		
	V. F. Kroupa (A specially written paper for this volume).	<b>367</b>

<b>Author Index</b>	<b>373</b>
<b>Subject Index</b>	<b>375</b>
<b>About the Editor</b>	<b>383</b>