

To my parents

B. Bala Tripura Sundari

To Ravi and Chandra

T.R. Padmanabhan



# CONTENTS

<i>PREFACE</i> .....	<i>xi</i>
<i>ACKNOWLEDGEMENTS</i> .....	<i>xiii</i>
<b>1 INTRODUCTION TO VLSI DESIGN</b> .....	<b>1</b>
1.1 INTRODUCTION .....	1
1.2 CONVENTIONAL APPROACH TO DIGITAL DESIGN .....	1
1.3 VLSI DESIGN .....	3
1.4 ASIC DESIGN FLOW .....	4
1.5 ROLE OF HDL .....	9
<b>2 INTRODUCTION TO VERILOG</b> .....	<b>11</b>
2.1 VERILOG AS AN HDL .....	11
2.2 LEVELS OF DESIGN DESCRIPTION .....	11
2.3 CONCURRENCY .....	13
2.4 SIMULATION AND SYNTHESIS .....	14
2.5 FUNCTIONAL VERIFICATION .....	14
2.6 SYSTEM TASKS .....	16
2.7 PROGRAMMING LANGUAGE INTERFACE (PLI) .....	16
2.8 MODULE .....	16
2.9 SIMULATION AND SYNTHESIS TOOLS .....	22
2.10 TEST BENCHES .....	27
<b>3 LANGUAGE CONSTRUCTS AND CONVENTIONS IN VERILOG</b> .....	<b>31</b>
3.1 INTRODUCTION .....	31
3.2 KEYWORDS .....	31
3.3 IDENTIFIERS .....	32
3.4 WHITE SPACE CHARACTERS .....	33
3.5 COMMENTS .....	33
3.6 NUMBERS .....	34
3.7 STRINGS .....	36
3.8 LOGIC VALUES .....	38
3.9 STRENGTHS .....	39
3.10 DATA TYPES .....	40
3.11 SCALARS AND VECTORS .....	41
3.12 PARAMETERS .....	42

3.13 MEMORY .....	43
3.14 OPERATORS .....	43
3.15 SYSTEM TASKS .....	44
3.16 EXERCISES .....	46
<b>4 GATE LEVEL MODELING – 1</b>	<b>47</b>
4.1 INTRODUCTION .....	47
4.2 AND GATE PRIMITIVE .....	47
4.3 MODULE STRUCTURE .....	50
4.4 OTHER GATE PRIMITIVES .....	51
4.5 ILLUSTRATIVE EXAMPLES .....	51
4.6 TRI-STATE GATES .....	64
4.7 ARRAY OF INSTANCES OF PRIMITIVES .....	66
4.8 ADDITIONAL EXAMPLES .....	69
4.9 EXERCISES .....	79
<b>5 GATE LEVEL MODELING – 2</b>	<b>81</b>
5.1 INTRODUCTION .....	81
5.2 DESIGN OF FLIP-FLOPS WITH GATE PRIMITIVES .....	81
5.3 DELAYS .....	91
5.4 STRENGTHS AND CONTENTION RESOLUTION .....	102
5.5 NET TYPES .....	109
5.6 DESIGN OF BASIC CIRCUITS .....	115
5.7 EXERCISES .....	124
<b>6 MODELING AT DATA FLOW LEVEL</b>	<b>127</b>
6.1 INTRODUCTION .....	127
6.2 CONTINUOUS ASSIGNMENT STRUCTURES .....	127
6.3 DELAYS AND CONTINUOUS ASSIGNMENTS .....	133
6.4 ASSIGNMENT TO VECTORS .....	135
6.5 OPERATORS .....	136
6.6 ADDITIONAL EXAMPLES .....	150
6.7 EXERCISES .....	157
<b>7 BEHAVIORAL MODELING — 1</b>	<b>159</b>
7.1 INTRODUCTION .....	159
7.2 OPERATIONS AND ASSIGNMENTS .....	160
7.3 FUNCTIONAL BIFURCATION .....	161
7.4 INITIAL CONSTRUCT .....	164
7.5 ALWAYS CONSTRUCT .....	168
7.6 EXAMPLES .....	170
7.7 ASSIGNMENTS WITH DELAYS .....	184
7.8 wait CONSTRUCT .....	192
7.9 MULTIPLE ALWAYS BLOCKS .....	195

7.10 DESIGNS AT BEHAVIORAL LEVEL .....	197
7.11 BLOCKING AND NONBLOCKING ASSIGNMENTS .....	201
7.12 THE <i>case</i> STATEMENT .....	205
7.13 SIMULATION FLOW .....	214
7.14 EXERCISES .....	217
<b>8 BEHAVIORAL MODELING II</b> .....	<b>219</b>
8.1 INTRODUCTION .....	219
8.2 <i>if</i> AND <i>if-else</i> CONSTRUCTS .....	219
8.3 <i>assign-deassign</i> CONSTRUCT .....	225
8.4 <i>repeat</i> CONSTRUCT .....	236
8.5 <i>for</i> LOOP .....	238
8.6 THE <i>disable</i> CONSTRUCT .....	244
8.7 <i>while</i> LOOP .....	249
8.8 <i>forever</i> LOOP .....	254
8.9 PARALLEL BLOCKS .....	258
8.10 <i>force-release</i> CONSTRUCT .....	261
8.11 EVENT .....	266
8.12 EXERCISES .....	268
<b>9 FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES</b> .....	<b>273</b>
9.1 INTRODUCTIUON .....	273
9.2 FUNCTION .....	273
9.3 TASKS .....	286
9.4 USER-DEFINED PRIMITIVES (UDP) .....	292
9.5 EXERCISES .....	302
<b>10 SWITCH LEVEL MODELING</b> .....	<b>305</b>
10.1 INTRODUCTION .....	305
10.2 BASIC TRANSISTOR SWITCHES .....	305
10.3 CMOS SWITCH .....	318
10.4 BIDIRECTIONAL GATES .....	328
10.5 TIME DELAYS WITH SWITCH PRIMITIVES .....	333
10.6 INSTANTIATIONS WITH STRENGTHS AND DELAYS .....	334
10.7 STRENGTH CONTENTION WITH TRIREG NETS .....	334
10.8 EXERCISES .....	337
<b>11 SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES</b> .....	<b>339</b>
11.1 INTRODUCTION .....	339
11.2 PARAMETERS .....	339
11.3 PATH DELAYS .....	348
11.4 MODULE PARAMETERS .....	371
11.5 SYSTEM TASKS AND FUNCTIONS .....	373
11.6 FILE-BASED TASKS AND FUNCTIONS .....	383

11.7 COMPILER DIRECTIVES .....	385
11.8 HIERARCHICAL ACCESS .....	393
11.9 GENERAL OBSERVATIONS .....	404
11.10 EXERCISES .....	405
<b>12 QUEUES, PLAS, AND FSMS</b> .....	<b>407</b>
12.1 INTRODUCTION .....	407
12.2 QUEUES .....	407
12.3 PROGRAMMABLE LOGIC DEVICES (PLDs) .....	414
12.4 DESIGN OF FINITE STATE MACHINES .....	418
12.5 EXERCISES .....	433
APPENDIX A (Keywords and Their Significance) .....	443
APPENDIX B (Truth Tables of Gates and Switches) .....	447
REFERENCES .....	449
INDEX .....	451