
Contents

About the Author	xvii
Preface	xix
Acknowledgments	xxiii
1 Failure Analysis and ESD	1
1.1 Introduction	1
1.1.1 FA Techniques for Evaluation of ESD Events	2
1.1.2 Fundamental Concepts of ESD FA Methods and Practices	3
1.1.3 ESD Failure: Why Do Semiconductor Chips Fail?	4
1.1.4 How to Use FA to Design ESD Robust Technologies	5
1.1.5 How to Use FA to Design ESD Robust Circuits	6
1.1.6 How to Use FA for Temperature Prediction	7
1.1.7 How to Use Failure Models for Power Prediction	8
1.1.8 FA Methods, Design Rules, and ESD Ground Rules	9
1.1.9 FA and Semiconductor Process-Induced ESD Design Asymmetry	9
1.1.10 FA Methodology and Electro-thermal Simulation	10
1.1.11 FA and ESD Testing Methodology	10
1.1.12 FA Methodology for Evaluation of ESD Parasitics	13
1.1.13 FA Methods and ESD Device Operation Verification	14
1.1.14 FA Methodology to Evaluate Inter-power Rail Electrical Connectivity	14
1.1.15 How to Use FA to Eliminate Failure Mechanisms	16
1.2 ESD Failure: How Do Micro-electronic Devices Fail?	16
1.2.1 ESD Failure: How Do Metallurgical Junctions Fail?	18
1.2.2 ESD Failure: How Do Insulators Fail?	18
1.2.3 ESD Failure: How Do Metals Fail?	19
1.3 Sensitivity of Semiconductor Components	20
1.3.1 ESD Sensitivity as a Function of Materials	20
1.3.2 ESD Sensitivity as a Function of Semiconductor Devices	21
1.3.3 ESD Sensitivity as a Function of Product Type	21

viii CONTENTS

1.3.4	ESD and Technology Scaling	22
1.3.5	ESD Technology Roadmap	24
1.4	How Do Semiconductor Chips Fail—Are the Failures Random or Systematic?	24
1.5	Closing Comments and Summary	26
	Problems	26
	References	27
2	Failure Analysis Tools, Models, and Physics of Failure	31
2.1	FA Techniques for Evaluation of ESD Events	31
2.2	FA Tools	34
2.2.1	Optical Microscope	34
2.2.2	Scanning Electron Microscope	35
2.2.3	Transmission Electron Microscope	35
2.2.4	Emission Microscope	35
2.2.5	Thermally Induced Voltage Alteration	36
2.2.6	Superconducting Quantum Interference Device Microscope	37
2.2.7	Atomic Force Microscope	38
2.2.8	The 2-D AFM	40
2.2.9	Picosecond Current Analysis Tool	40
2.2.10	Transmission Line Pulse—Picosecond Current Analysis Tool	42
2.3	ESD Simulation: ESD Pulse Models	43
2.3.1	Human Body Model	43
2.3.2	Machine Model	44
2.3.3	Cassette Model	45
2.3.4	Socketed Device Model	46
2.3.5	Charged Board Model	46
2.3.6	Cable Discharge Event	47
2.3.7	IEC System-Level Pulse Model	49
2.3.8	Human Metal Model	50
2.3.9	Transmission Line Pulse Testing	51
2.3.10	Very Fast Transmission Line Pulse (VF-TLP) Model	53
2.3.11	Ultra-fast Transmission Line Pulse (UF-TLP) Model	53
2.4	Electro-Thermal Physical Models	54
2.4.1	Tasca Model	54
2.4.2	Wunsch–Bell Model	56
2.4.3	Smith–Littau Model	60
2.4.4	Ash Model	62
2.4.5	Arkihfov, Astvatsaturyan, Godovosyn, and Rudenko Model	63
2.4.6	Dwyer, Franklin, and Campbell Model	63
2.4.7	Vlasov–Sinkevitch Model	67
2.5	Statistical Models for ESD Prediction	68
2.6	Closing Comments and Summary	70
	Problems	70
	References	71

3 CMOS Failure Mechanisms	77
3.1 Tables of CMOS ESD Failure Mechanisms	77
3.2 LOCOS Isolation-Defined CMOS	77
3.2.1 LOCOS-Bound Structures	82
3.2.2 LOCOS-Bound P ⁺ /N-well Junction Diode	83
3.2.3 LOCOS-Bound N ⁺ /P ⁻ Substrate Junction Diode	84
3.2.4 LOCOS-Bound N-well/P ⁻ Substrate Junction Diode	84
3.2.5 LOCOS-Bound Lateral N-well to N-well	85
3.2.6 LOCOS-Bound Lateral N ⁺ to N-well	85
3.2.7 LOCOS-Bound Lateral PNP Bipolar	85
3.2.8 LOCOS-Bound Thick Oxide MOSFET	85
3.3 Shallow Trench Isolation (STI)	86
3.3.1 STI Pull-down ESD Failure Mechanism	86
3.3.2 STI Pull-down and Gate Wrap-around	87
3.3.3 Silicides and Diodes	88
3.3.4 Non-silicide Diode Structures	88
3.3.5 STI-Defined P ⁺ /N-well Diode	88
3.3.6 STI-Defined N-well to Substrate Diode	88
3.3.7 STI Lateral N-well to N-well NPN Structures	90
3.4 Polysilicon-Defined Devices	90
3.4.1 Polysilicon-Bound Gated Diode	91
3.5 Lateral Diode with Block Mask	92
3.6 MOSFETs	92
3.6.1 N-channel MOSFETs	93
3.6.2 N-channel Multi-finger MOSFETs	95
3.6.3 Cascoded Series N-channel MOSFETs	97
3.6.4 P-channel MOSFETs	97
3.6.5 P-channel Multi-finger MOSFETs	98
3.6.6 Tungsten Silicide Gate MOSFET	98
3.6.7 Polysilicon Silicide Gate MOSFET	98
3.6.8 Metal Gate/High <i>k</i> Dielectric MOSFET	98
3.7 Resistors	99
3.7.1 Diffused Resistors	99
3.7.2 N-well Resistors	99
3.7.3 Buried Resistors	101
3.7.4 Silicide Blocked N-diffusion Resistors	102
3.8 Interconnects: Wires, Vias, and Contacts	102
3.8.1 Aluminum Interconnects	103
3.8.2 Copper Interconnects	104
3.8.3 Tungsten Interconnects	107
3.8.4 Vias	107
3.8.5 Contacts	110
3.9 ESD Failure in CMOS Nanostructures	112
3.9.1 ESD Failures in 130 nm Technology	112
3.9.2 ESD Failures in 90 nm Technology	113
3.9.3 ESD Failures in 65 nm Technology	114

x CONTENTS

3.9.4	ESD Failures in 45 nm Technology	115
3.9.5	ESD Failures in 32 nm Technology	115
3.9.6	ESD Failures in 22 nm Technology	116
3.10	Closing Comments and Summary	118
	Problems	118
	References	119
4	CMOS Circuits: Receivers and Off-Chip Drivers	125
4.1	Tables of CMOS Receiver and OCD ESD Failure Mechanisms	125
4.2	Receiver Circuits	125
4.3	Receivers Circuits with ESD Networks	127
4.3.1	Receiver with Dual Diode and Series Resistor	127
4.3.2	Receiver with Diode–Resistor–Diode	128
4.3.3	Receiver with Diode–Resistor–MOSFET	128
4.4	Receiver Circuits with Half-Pass Transmission Gate	131
4.5	Receiver with Full-Pass Transmission Gate	134
4.5.1	Receiver with Full-Pass Transmission Gate with Second Power Source	135
4.6	Receiver, Half-Pass Transmission Gate, and Keeper Network	135
4.6.1	Receiver, Half-Pass Transmission Gate, and the Modified Keeper Network	138
4.7	Receiver Circuits with Pseudo-Zero V_T Half-Pass Transmission Gate	139
4.8	Receiver with Zero V_T Transmission Gate	141
4.9	Receiver Circuits with Bleed Transistors	143
4.10	Receiver Circuits with Test Functions	144
4.11	Receiver with Schmitt Trigger Feedback Networks	146
4.12	Off-Chip Drivers	148
4.12.1	OCD Design Process-Related ESD Failure	148
4.13	Single NFET Pull-down OCD	149
4.14	Series Cascode MOSFETs	150
4.15	I/O Design Considerations and ESD Parasitic Failure Mechanisms	152
4.15.1	Layout-Dependent ESD Failure Mechanisms	153
4.16	Closing Comments and Summary	155
	Problems	155
	References	156
5	CMOS Integration	159
5.1	Table of CMOS Integration ESD Failure Mechanisms	159
5.2	Architecture and Design Synthesis-Related Failures	159
5.3	Alternate Current Loop	161
5.4	Chip Capacitance	161
5.5	ESD Power Clamps	161
5.6	Intra- and Inter-domain ESD Protection	162
5.7	Split Ground Configurations	162

5.8	Mixed Voltage Interface	163
5.8.1	Peripheral V_{CC} and Core V_{DD} Power Rails	163
5.8.2	Two Power Supply: Peripheral and Core V_{DD} Power Rails	164
5.8.3	Voltage Regulators	166
5.9	Mixed Signal Interface	168
5.9.1	Digital and Analog	168
5.9.2	Digital, Analog, and RF	169
5.10	Inter-domain Signal Line ESD Failures	170
5.10.1	Digital-to-Analog Signal Line Failures	170
5.11	Decoupling Capacitors	173
5.12	System Clock and Phase-Locked Loop	174
5.13	Fuse Networks	174
5.13.1	Fuse Networks and ESD Failure Mechanisms	174
5.13.2	eFUSE and ESD Failure Mechanisms	176
5.14	Bond Pads	178
5.14.1	Floating Bond Pads	178
5.14.2	Floating Bond Pads over Interconnects	179
5.14.3	Bond Pad Failure: Programmable V_{DD}	180
5.14.4	Bond Pad to Bond Pad ESD Failures	180
5.14.5	Bond Pad Failure: ESD Structures under Bond Pads	181
5.15	MOSFET Gate Structure	181
5.15.1	MOSFET Floating Gate and Floating Gate Tie Down	181
5.15.2	MOSFET Gates Connected to Power V_{DD}	182
5.16	Fill Shapes	182
5.17	No Connects	182
5.18	Test Circuitry	183
5.19	Multi-chip Systems	183
5.19.1	Multi-chip Systems on Multi-layer Ceramic	183
5.19.2	Multi-chip Systems and Silicon Carriers	184
5.19.3	Multi-chip Systems: Chip-to-Chip Failures with Adjacent Chips	184
5.19.4	Multi-chip Systems: Proximity Communications	185
5.20	CMOS Latchup Failures	185
5.20.1	Table of Latchup Failures	185
5.20.2	Latchup Failure Mechanisms	187
5.21	Closing Comments and Summary	188
	Problems	189
	References	191
6	SOI ESD Failure Mechanisms	195
6.1	Tables of SOI Device and Integration ESD Failure Mechanisms	195
6.2	SOI N-channel MOSFETs	197
6.2.1	SOI Single-Finger N-channel MOSFETs	197
6.2.2	SOI Multi-finger MOSFETs	198

xii CONTENTS

6.3	SOI Diodes	199
6.3.1	SOI Poly-bound Gated Diode	199
6.3.2	SOI Poly-bound Gated Diode with Halo Implants	199
6.4	SOI Buried Resistors	201
6.5	SOI Failure Mechanisms in 150 nm Technology	202
6.5.1	Lateral Graded Gated SOI Diode Structure	203
6.5.2	Lateral Ungated SOI Diode Structure	203
6.6	SOI ESD Failure Mechanisms in 45 nm Technology	204
6.6.1	SOI Lateral Gated Diode	204
6.6.2	SOI Double-Well Field Effect Device	204
6.6.3	SOI: ESD under BOX	205
6.7	SOI ESD Failure Mechanisms in 32 nm Technology	206
6.8	SOI ESD Failure Mechanisms in 22 nm Technology and the Future	207
6.9	SOI Design Synthesis and ESD Failure Mechanisms	210
6.9.1	SOI ESD Circuit Failure Mechanisms	210
6.9.2	Mixed Voltage SOI ESD Circuit Failure Mechanisms	212
6.9.3	SOI Receiver Network ESD Failures	214
6.9.4	SOI Fuse Networks	215
6.9.5	SOI Dynamic Threshold Circuitry	215
6.9.6	SOI Active Clamp Circuitry	216
6.10	SOI Integration: ESD Failure Mechanisms	217
6.11	Closing Comments and Summary	218
	Problems	218
	References	220
7	RF CMOS and ESD	225
7.1	Tables of RF CMOS ESD Failure Mechanisms	225
7.2	RF MOSFET	228
7.3	RF Shallow Trench Isolation Diode	229
7.4	RF Polysilicon Gated Diode	231
7.5	Silicon-Controlled Rectifier	232
7.6	Schottky Barrier Diodes	233
7.7	Capacitors	235
7.7.1	MIM Capacitor	236
7.7.2	Varactors and Hyper-abrupt Varactor Capacitors	237
7.7.3	Metal-ILD-Metal Capacitor	237
7.7.4	VPP Capacitor	237
7.7.5	Decoupling Capacitor	241
7.8	Resistors	241
7.8.1	Silicon Resistors	241
7.8.2	Polysilicon Resistors	241
7.8.3	Electronic Fuse (eFUSE) Resistor	241
7.9	Inductors	244
7.9.1	Planar Inductors	245
7.9.2	T-coil Inductor Pairs	248

7.10	Examples of RF ESD Circuit Failure Mechanisms	250
7.11	Closing Comments and Summary	253
	Problems	253
	Reference	254
8	Micro-electromechanical Systems	259
8.1	Table of MEM Failure Mechanisms	260
8.2	Electrostatically Actuated Devices	260
8.3	Micro-mechanical Engines	263
8.4	Torsional Ratcheting Actuator	265
8.5	Electromagnetic Micro-power Generators	267
8.6	MEM Inductors	269
8.7	Electrostatically Actuated Variable Capacitor	270
8.8	Micro-mechanical Switches	271
8.9	RF MEM Switch	271
8.10	Micro-mechanical Mirrors	277
8.11	Electrostatically Actuated Torsional Micro-mirrors	277
8.12	Closing Comments and Summary	281
	Problems	281
	References	282
9	Gallium Arsenide	287
9.1	Tables of GaAs-Based ESD Failure Mechanisms	287
9.2	GaAs Technology	290
9.3	GaAs Energy-to-failure and Power-to-failure	290
9.4	GaAs ESD Failures in Active and Passive Elements	293
9.5	GaAs HBT Devices	294
	9.5.1 GaAs HBT Device ESD Results	295
	9.5.2 GaAs HBT Diode Strings	296
9.6	GaAs HBT-Based Passive Elements	297
	9.6.1 GaAs HBT Base–Collector Varactor	297
9.7	GaAs PHEMT Devices	298
	9.7.1 GaAs PHEMT Low Noise Amplifiers	299
9.8	GaAs Power Amplifiers	300
	9.8.1 GaAs PAs with Off-Chip Protection	303
9.9	InGaAs	303
	9.9.1 InGaAs/AlGaAs PHEMT Devices	304
	9.9.2 InGaAs/AlGaAs PHEMT ESD Failure	305
9.10	Gallium Nitride	306
	9.10.1 GaN ESD Failure Mechanisms	307
9.11	InP and ESD	309
9.12	Closing Comments and Summary	309
	Problems	309
	References	310

10 Smart Power, LDMOS, and BCD Technology	315
10.1 Tables of LDMOS ESD Failure Mechanisms	315
10.2 LOCOS-Defined LDMOS Devices	317
10.3 STI-Defined LDMOS Devices	319
10.4 STI-Defined Isolated LDMOS Transistors	320
10.5 LDMOS Transistors: ESD Electrical Measurements	321
10.6 LDMOS-Based ESD Networks	322
10.7 LDMOS ESD Failure Mechanisms	323
10.8 LDMOS Transistor Design Enhancement	324
10.9 Latchup Events in LDMOS and BCD Technology	324
10.10 Closing Comments and Summary	326
Problems	327
References	328
11 Magnetic Recording	333
11.1 Tables of Magnetic Recording Failure Mechanisms	333
11.2 MR Heads	334
11.2.1 MR Head Structure	335
11.2.2 MR Head Electrical Model	336
11.2.3 MR Head ESD Failures	337
11.2.4 AMR Head Failure Mechanisms	340
11.2.5 ESD Protection of MR Head	342
11.3 Inductive Heads	343
11.3.1 Inductive Head Structure	343
11.3.2 Inductive Head Structure: Electrical Schematic	344
11.3.3 Inductive Head Structure: ESD Failures	345
11.4 GMR Heads	346
11.4.1 GMR Head Structure	346
11.4.2 GMR Head ESD Failures	347
11.4.3 GMR Head ESD Protection	347
11.5 TMR Heads	349
11.5.1 TMR Structure	349
11.5.2 TMR ESD Results	349
11.5.3 TMR ESD Failure Mechanisms	351
11.6 ESD Solutions	351
11.6.1 Inductive Head Shunt	351
11.6.2 MR Shunt	351
11.6.3 Parasitic Magnetic Shields	352
11.6.4 Suspension ESD Shunt	352
11.6.5 Integration of a Silicon Chip	353
11.6.6 Deposited Amorphous Silicon ESD Diodes	353
11.6.7 Silicon Substrates	353
11.7 Closing Comments and Summary	354
Problems	354
References	355

12 Photo-masks and Reticles: Failure Mechanisms	361
12.1 Table of Photo-masks Failure Mechanisms	361
12.2 Photo-mask Failure Mechanisms	361
12.3 Photo-mask Inspection Tools	364
12.4 Photo-mask ESD Characterization	365
12.5 Electrical Breakdown versus Gap Spacing	365
12.6 Electrical Breakdown in Air: The Townsend Model	367
12.7 Electrical Breakdown in Air: Toepler's Spark Law	367
12.8 Air Breakdown: The Paschen Breakdown Model	367
12.9 Paschen Curve versus Reticle Breakdown Plot	368
12.10 Electrical Model of Photo-mask Breakdown	369
12.11 ESD Latent Damage	371
12.12 ESD Damage for Single versus Multiple Events	372
12.13 ESD Damage to Anti-reflective Coating	373
12.14 ESD Solutions in Photo-masks	373
12.15 Closing Comments and Summary	375
Problems	375
References	376
Index	379

