1 Epitaxial Thin Film Crystalline Silicon Solar Cells on low Cost Silicon Carriers

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1.1 INTRODUCTION

In order to substantially reduce the costs of present crystalline Si solar cells, the material consumption of highly pure Si in a typical solar cell structure should be reduced. Most of the crystalline Si material merely acts as a mechanical carrier for the solar cell device with most of the optical absorption taking place in the upper 30 μm region. When special care is taken to maximize optical confinement active layer thicknesses as low as 0.5 μm would be sufficient [1] for reaching energy conversion efficiencies above 15 %. Moving to thinner Si wafers to reduce Si consumption represents one option, but there are obvious concerns about process yield, showing up when producing cells in Si-wafers with thicknesses below 200 μm. Special substrate types, specifically developed to avoid crack propagation, like the tri-crystalline Si material [2] or thin edge film growth (EFG) ribbons [3], might alleviate this problem.

A more ambitious approach to reduce solar cell costs consists of growing a thin active crystalline Si layer onto a cheap carrier. This carrier can be a ceramic substrate or even a glass substrate when the deposition and solar cell process are performed at low temperature. The Si layer, deposited on top of these substrates, will be micro- or polycrystalline with a grain size determined by the growth temperature and supersaturation conditions during the silicon layer deposition. For microcrystalline Si solar cells on glass, exhibiting grain sizes in the range 1–100 nm, energy conversion efficiencies[1] up to 10 % are reported [4]. On the other hand, it turns out to be difficult to realize solar cells with proper energy conversion efficiencies in material with a grain size of 1–10 μm [5, 6], although substantial progress has been made lately in this field [7]. On ceramic substrates, which withstand high temperatures, liquid phase recrystallization [8, 9], is often applied to increase the final grain size, whereas laser recrystallization and rapid thermal annealing is being developed for substrates which can only withstand process temperatures >650 °C for a limited time [10, 11].

[1] In the remainder of the chapter energy conversion efficiency will be named "efficiency"

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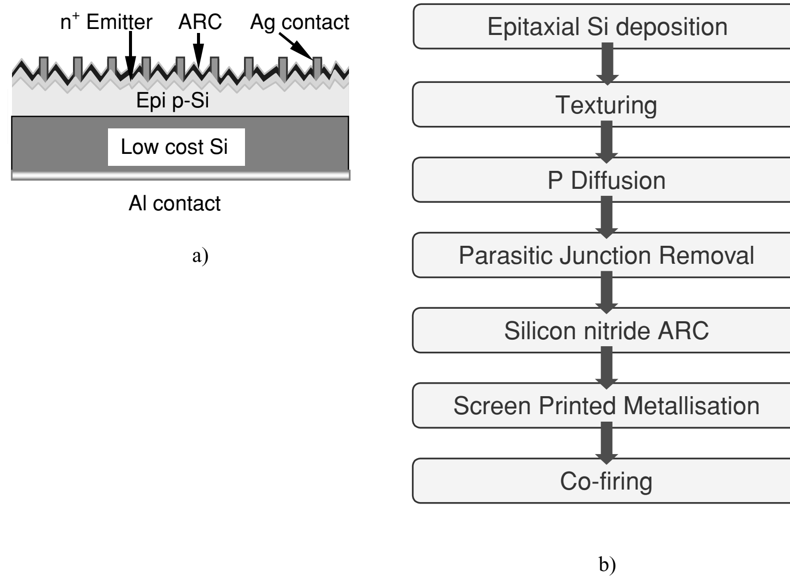

Figure 1.1 a) Schematic cross-section of epitaxial solar cell structure; b) Comparison of generic industrial process flows for epitaxial solar cells versus self-supporting crystalline Si solar cells; only the first process step (the epitaxial deposition) would be added to the normal process flow for industrial crystalline Si solar cells.

The basic idea behind the thin film approach discussed in this chapter, is the realization of a thin crystalline Si film of high electronic quality [12, 13] on a low cost Si carrier substrate by means of epitaxial growth. When discussing thin film solar cell technologies, thin film crystalline Si solar cells, based on an epitaxially grown active layer on an inactive highly doped low cost Si carrier substrate[2] are often left untreated. This is readily understood when looking at Figure 1.1a, showing the generic structure of the type of the solar cell being discussed within this chapter. The depicted structure strongly resembles the structure of a classical, self supporting bulk crystalline Si solar cell and, as a result, the basic solar cell process to produce the solar cell is very similar to the practices used within the photovoltaics (PV) industry nowadays. This is, at the same time, the strongest and weakest point of this technology. Its structural similarity would result in a low acceptance threshold in the solar cell industry, which is presently based at 95 % on crystalline Si. Indeed, the only major change required to introduce this technology within the crystalline Si PV industry would be the introduction of a high throughput epitaxial Si deposition reactor at the beginning of the production line as shown in Figure 1.1b. In this way, additional investments and risks can be minimized, which is a nonnegligible element in major investment decisions.[3] In this context one sometimes uses the term ‘wafer equivalents’ to emphasize the similarity aspect. Last, but not least, the ‘wafer scale’ approach has the advantage that process yield can be kept at a high level using the in-line

[2] In the remainder of the chapter the shorter term “epitaxial Si solar cells”, will be used, although this is not the only thin-film crystalline technology in which an epitaxial Si layer is being deposited during the formation of the active layer.
[3] The large investment when building thin-film solar cell production lines is often mentioned as a major barrier.

production quality monitoring tools available in crystalline Si production lines. For thin film solar cell technologies which are depositing the active layers on large area substrates of more than 1 m^2, the uniformity and reproducibility requirements are much more severe to obtain a similar yield.

The similarity of the basic epitaxial solar cell structure to classical crystalline Si solar cells also creates the impression that the potential cost savings by using this epitaxial cell technology would be marginal. A closer look reveals that this is not necessarily true. As mentioned in the introductory chapter of this book, when analyzing the cost structure of multicrystalline Si solar cell modules, one sees that more than 50 % of the module cost consists of costs related to the crystalline Si substrate [14, 15]. At the time of redaction of this chapter there is a tendency for the crystalline Si substrate costs to increase as one is facing a situation of scarcity of poly-Si feedstock material. This is temporary in to the author's opinion, because of major investments in additional poly-Si feedstock production specifically tuned to the needs of the Si solar cell industry [16]. Nevertheless, it remains that the cost projections for this specific 'solar grade' poly-Si feedstock material are mostly in the range 15–20 € /kg. Based on such a feedstock cost and a further reduction in the amount of crystalline Si/Watt peak (W_p) in line with the historical trend of 5 %/year [17] the cost of bulk crystalline Si solar cell modules would be in the range of 1.2 $/$W_p$ with industrial efficiencies near 20 % [15]. The epitaxial cell route is based on metallurgical or upgraded metallurgical grade Si substrate material which would cost less than 5 € /kg.[4] In the situation of having a high throughput epitaxial Si deposition process with costs below 10 € /m^2, the final cost of the module would be in the range 0.9–1 $/$W_p$, even with an cell efficiency of only 15 %. Besides this cost potential, the epitaxial cell approach would also render the PV industry independent from any supply issues on the level of poly-Si feedstock material.

The substrates of interest for epitaxial Si solar cells are low cost Si substrates which, because of their doping and impurity levels, do not allow the realization of a solar cell with sufficient efficiency within the substrate. The Si substrate can be a highly doped Si ribbon; see e.g. [18] for chemical vapor deposition (CVD)-grown epitaxial cells on an ribbon growth on substrate (RGS) ribbon or [19, 20] for an liquid phase epitaxy (LPE)-grown layer on the same ribbon type. Also Si substrates from metallurgical grade Si (MG-Si) or upgraded metallurgical grade Si (UMG-Si) ingots are an attractive option [13, 21, 22]. By growth of an epitaxial layer with suitable doping and reduced impurity levels on top of this substrate, a better performing solar cell can be realized on top of this substrate [21]. The secondary ion mass spectrometry (SIMS) profile, shown in Figure 1.2, illustrates that the epitaxial layer on top of the contaminated substrate does indeed contain a substantially lower content of impurities than the substrate.

The objective of this chapter is to outline the different epitaxial cell approaches to the level of deposition technology and epitaxial layer structure. The solar cell process developments will only be discussed insofar as the solar cell results shed more light on the efficiency potential in laboratory conditions or in an industrial environment. Specific attention will be given to those aspects which have to be developed to make the epitaxial cell technology viable for industrial production. The latter aspect does not only concern the concepts and development of high throughput deposition technologies and adaptation of solar cell processes but also covers the

[4] Si as such is not a rare material and the reduction of sand to metallurgical grade is consistent with a cost of 1–2 Euro/kg.

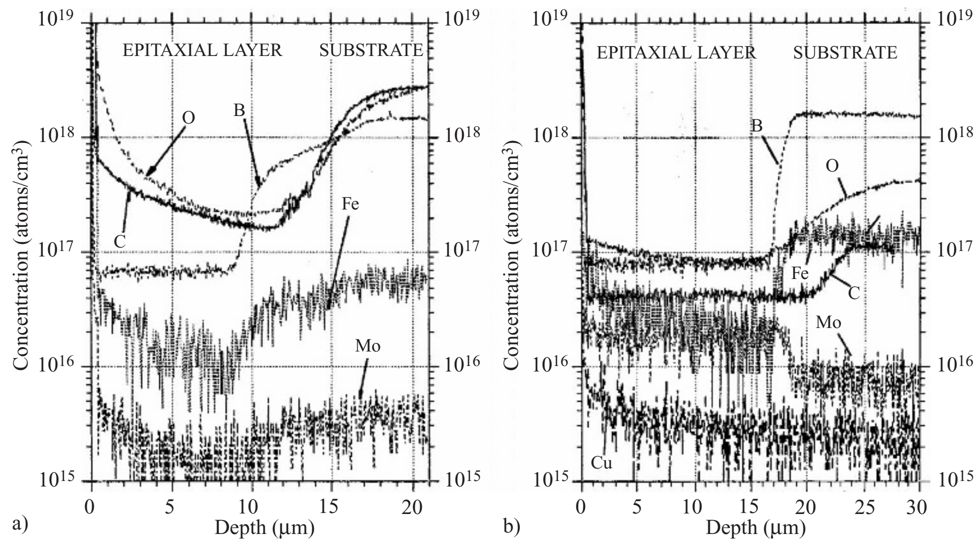

Figure 1.2 SIMS profiles of the impurities O, C, Fe, Mo, Cu in epitaxial layer on a) highly doped multicrystalline Si substrate (SILSO); and b) on a MG-Si substrate. Note the decreasing impurity concentrations in the epitaxial layer for Fe, O and C in both cases.

approaches to keeping the epitaxial layer thickness as low as possible. This can only be realized by enhanced light absorption and/or optical confinement of light within the active volume of the cell. Concerning optical confinement, the reader will immediately remark that this is a difficult issue as the substrate and active material are both crystalline Si, which excludes major reflection of light at the interface between the Si substrate and the active layer. To solve this intrinsic problem innovative schemes based on a buried reflector are required. The different approaches to realizing such a buried reflector will be discussed. Alloying with Ge is one other possibility to enhance the cell's absorbance.

1.2 DEPOSITION TECHNOLOGIES

The different deposition technologies by which epitaxial layers for solar cell applications can be grown are discussed as a function of deposition temperature, starting from the technique using the highest deposition temperature. This classification methodology also reflects the amount of experimental results and the maturity of the respective techniques. This is not a surprising finding since the epitaxial layers needed for epitaxial solar cells are quite thick in comparison with the typical layer thickness needed for other electronic applications (with the exception of epitaxial layers for power devices). The required epitaxial layer thickness which is in the range 5–30 μm requires a high growth rate to avoid excessive deposition times. At lower deposition temperatures the adatom surface mobility decreases resulting in an increasing number of crystallographic defects because the adatoms do not have sufficient time to relax into the lattice sites. As a result, at lower temperatures additional energy besides the thermal energy has to be supplied to increase the surface mobility and to allow high-quality epitaxial growth. This additional energy can supplied by means of accelerated ions or through plasma techniques.

1.2.1 Thermally assisted chemical vapor deposition

The deposition technique, which has been and is still most widely studied in the context of epitaxial solar cells, is based on thermally assisted heterogeneous decomposition of a Si precursor and doping gases at a heated Si -surface. In the text it will be referred to as thermally assisted chemical vapor deposition (TA-CVD). Since the seventies attempts have been made to use this technique in the frame of solar cells [23] and nowadays it is still widely used in Europe [15, 24] and Japan [25] for the realization of thin film crystalline Si solar cells. There are numerous reactor types which have been used for TA-CVD. Batch type as well as single wafer systems have been used. Single wafer systems are often horizontal flow reactors, where gases are introduced at one end of a chamber and exit from the other end. The wafer either lies on a silicon carbide coated graphite susceptor, or is thermally isolated and heated only by radiation. In the latter case, extremely fast heating and cooling rates are achievable and the technique is therefore often referred to as rapid thermal CVD (RT-CVD) [26]. The technique was pioneered in the eighties [27] and the specific study of this technique for thin film crystalline Si solar cells was conducted in the laboratory of the Institut d'Electronique du Solide et des Systèmes (INESS, Strasbourg [26] (see Figure 1.3). It avoids unwanted Si deposition on the cool furnace walls and reduces the time associated with heating and cooling of the substrates with all the energy being used for heating of the substrate and not of the furnace periphery. Batch type multiwafer reactors include pancake and barrel reactors, where rotation of the wafers on flat or cylindrical substrate holders ensures the required uniformity and aerodynamic conditions, and low pressure CVD reactors (LPCVD).

CVD takes advantage of the large process expertise available in the field of microelectronics. The developed epitaxial deposition systems and processes allow highly reproducible and uniform layers, both on the level of thickness and of dopant control. Doping and thickness uniformity are typically in the range of a few % over areas as large as 200–300 mm. In fact, the specifications for microelectronic applications are much more severe than what is being aimed at in photovoltaic applications, where a uniformity requirement of about 10 % for thickness and doping levels is probably sufficient. Nevertheless TA-CVD has a number of inherent disadvantages in the frame of thin film crystalline Si solar cells. First of all, it uses Si precursors which are toxic and/or corrosive and these precursors represent obvious explosion risks. In addition, the temperatures needed to obtain high growth rates in the order of a few μm/min are in the range 1000–1200 °C.

The electronic quality of CVD-grown epitaxial layers has been studied by means of lifetime measurements with typical lifetimes found in the order of a few μs on monocrystalline Si reference substrates and in the order of 1 μs on multicrystalline substrates [28].

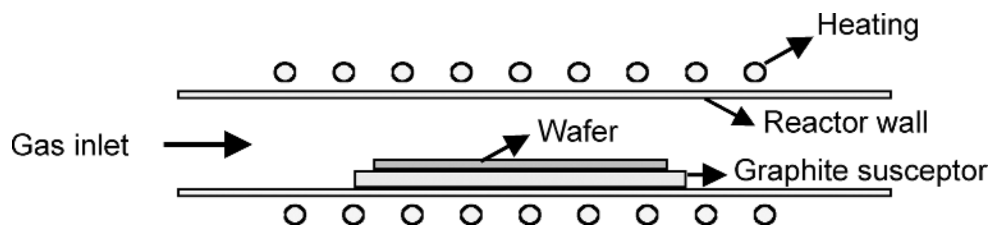

Figure 1.3 Schematic view of typical horizontal TA-CVD system (see reference [26]).

1.2.2 Liquid phase epitaxy – electrodeposition

A technique which is basically different from CVD in that it uses a liquid medium instead of a gaseous environment is solution growth (SG). The technique is also called liquid phase epitaxy (LPE) when this principle is used for the growth of epitaxial layers on a crystalline substrate [29]. In SG the growth of Si proceeds from a molten metal solution, typically Sn, In or sometimes Cu and Al [30, 31]. The molten metal is saturated with Si and afterwards slowly cooled. When cooling down, the melt gets supersaturated and the crystalline Si layer will be deposited from the melt onto a substrate by heterogeneous nucleation. The typical temperatures used range between 700 and 900 °C with growth rates in the order of 1 μm/min.

Besides its conceptual simplicity, the main advantage of the LPE technique lies in the fact that the growth system is close to thermal equilibrium and the Si atoms in the melt exhibit a large diffusion coefficient. Both factors enhance the crystallographic quality of the grown Si film. At the same time the close-to-equilibrium character also represents a serious drawback since nucleation of the Si-layer on a non-Si substrate or along defects at a Si surface becomes very difficult, which often results in non homogeneous and even nonconsistent Si layers on substrates containing crystallographic defects. In case of non-Si substrates like graphite this is often tackled by having a Si seed layer deposited by another technique. When growing epitaxial layers by the LPE technique on RGS [19] or silicon sheets from powder (SSP) ribbons [20] the epitaxial layer thickness in the region of the grain boundaries is often much reduced as compared to the intragrain thickness because the higher energy associated with the defects suppresses the layer growth near these defects, as schematically shown in Figure 1.4. In the regions where the epitaxial layer is much thinner, the n^+-emitter diffusion and p^+-substrate are in direct contact, resulting in leaky junctions and low fill factors. Faster cooling rates provide some improvement but the problem remains for uniform deposition over large areas.

Because of the low supersaturation during LPE growth, the defect density and excess carrier recombination activity in the LPE-grown epitaxial layers are lower as compared to CVD-grown layers. Numerous studies [32, 33] give strong support for this view. Electron beam induced current (EBIC) pictures of partially masked structures give unambiguous evidence of the reduced recombination in the LPE layers as shown in [32]. This reduction is caused by the tendancy to strive for the lowest energy configuration of the dislocation network in the LPE-layer. In addition, impurities will be contained in the molten metal solution because of the distribution coefficient between the liquid and solid phase. Minority-carrier lifetimes of several μs up to 10 μs have been reported in epitaxial layers for solar cells (see e.g. [34]).

A variation of solution growth is the electrodeposition of Si from molten salts (see Figure 1.5), which also allows the growth of epitaxial layers [35].

LPE allows one to easily incorporate an *in situ* doping gradient in the active base layer. The doping gradient will result in a positive electrical field in case of a decreasing dopant incorporation during growth. This positive field aids the collection of minority carriers and results in an increased effective diffusion length (L_{eff}) [36].

$$\frac{1}{L_{\mathrm{eff}}} = \frac{1}{2L}\left(\sqrt{\left(\frac{E}{E_c}\right)^2 + 4} - \frac{E}{E_c}\right) \tag{1.1}$$

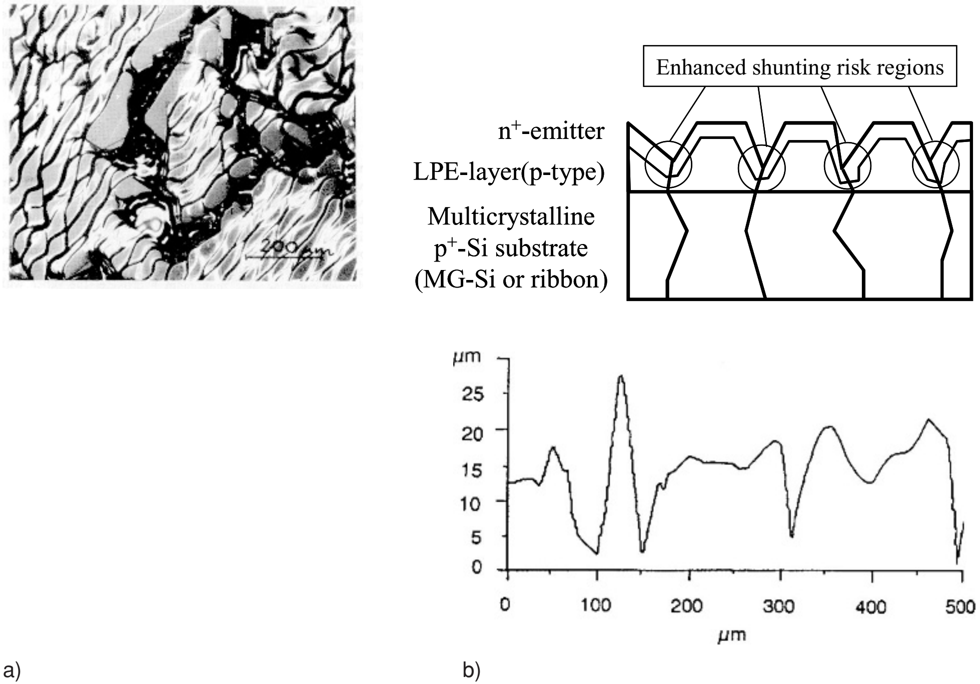

Figure 1.4 a) Picture and surface profile showing typical surface morphology of LPE-layer on defected Si substrate (taken from reference [19], courtesy of WIP, Munich, Germany); b) Schematic illustration of LPE growth topology problem in regions near crystallographic defects. It is obvious that during emitter diffusion, these regions are more susceptible to shunting between the n^+-emitter and the highly doped substrate.

with L the minority carrier diffusion length in the absence of an electrical field and

$$E_c = \frac{kT}{qL} \tag{1.2}$$

whereas E is given by:

$$E = \frac{kT}{qW_B} \ln\left(\frac{N_r}{N_f}\right) \tag{1.3}$$

where N_r represents the doping level at the substrate-epilayer interface and N_f is the doping level at the epilayer surface.

Intuitively one would expect a substantial performance increase by this effect. It was proven in [36] that the enhancement in most cases remains very limited and is only relevant in the absence of light trapping and with small minority-carrier diffusion lengths. It was recently pointed out by Majumdar *et al.* [37] that a negative field (i.e. the incorporation of the doping element increasing during the growth of the epitaxial layer) is a better approach. Although this result is to some extent counterintuitive, this can be understood from the consideration that the minority-carrier concentration gradient upon illumination is large anyway and is relatively

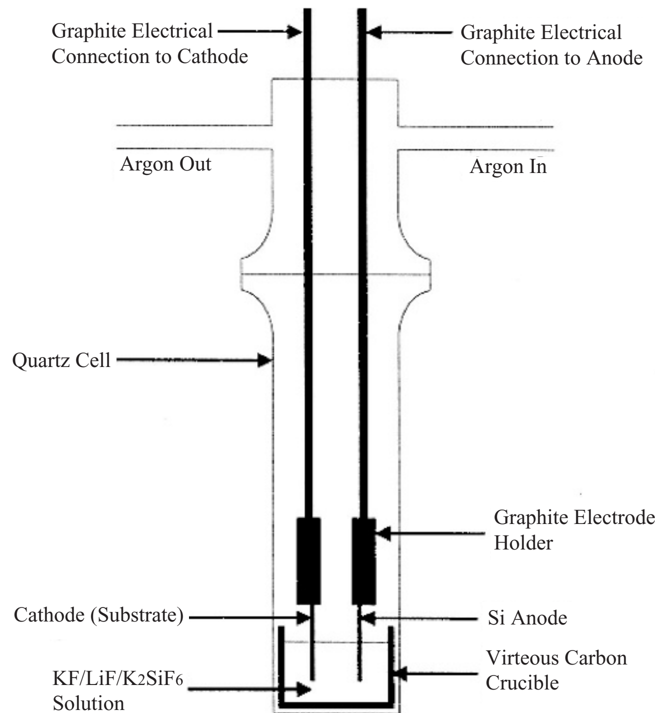

Figure 1.5 Schematic drawing of the electrodeposition technique. Reproduced Figure 1 with permission from J. T Moore, T. H. Wang, M. J. Heben, K. Douglas, T. F. Ciszek, 'Fused-salt electrodeposition of thin-layer silicon', Conference Record of the 26th IEEE Photovoltaic Specialists Energy Conference, Anaheim, 775, 1997. Copyright (1997) IEEE.

unaffected by the doping profile whereas the open circuit voltage is kept high because of the high base doping level near the junction.

1.2.3 Close space vapor transport technique

An alternative technique which yields very high chemical efficiencies[5] is based on so-called close space vapor transport [38]. Although the technique has been known since the sixties [39], it received renewed attention through research performed at the National Renewable Energy Laboratory (NREL), USA. A schematic drawing of this technique is shown in Figure 1.6. In this technique Si is transported from a source to a substrate. The driving force for the Si transfer is the temperature difference between both. A small separation between source and destination allows very high transfer efficiencies, because there is only limited loss of Si to the side walls. By means of this technique, epitaxial layers were deposited on highly doped mono- and multicrystalline Si substrates.

[5] The chemical efficiency describes the ratio between the Si-containing species incorporated in the growing solid Si film and the amount of Si supplied.

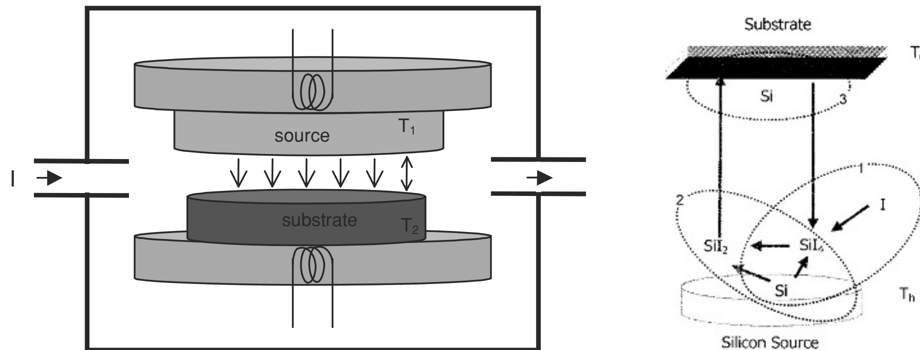

Figure 1.6 a) Schematic drawing of CVST technique for Si-deposition; b) Application of CSVT principle in the APIVT system presented in [38]. Reproduced Figure 1 with permission from T.H. Wang, T.F. Ciszek, M. Page, Y. Yan, R. Bauer, Q. Wang, J. Casey, R. Reedy, R. Matson, R. Ahrenkiel and M.M. Al-Jassim, 'Material properties of polysilicon layers deposited by atomspheric pressure iodine vapor transport', Conference Record of the twenty-eight IEEE Photovoltaic Specialists Conference, Anchorage 15–22 September 2000, p.138–141. Copyright (2000) IEEE.

The electronic quality obtained was remarkably good as evidenced by laboratory solar cells, made in these epitaxial atmospheric pressure iodine vapor transport (APIVT)-grown layers, especially taking into account the elevated deposition rate at a relatively low substrate temperature. The growth rate obtained at substrate temperatures in the range 650–850 °C (with the source temperature kept at 1300 °C) was in the order of 1–3 μm/min and was relatively insensitive to the substrate temperature. A model was constructed to explain this atypical temperature dependence of growth rate. The model incorporates the arrival rate of SiI_2, the departure rate of SiI_4 and surface migration and resulted in an expression for the growth rate R in the form:

$$R \propto (T - T_{\text{source}})\left(T_{\text{source}}^2 - T^2\right)\exp\left(\frac{-Q}{kT}\right) \tag{1.4}$$

with T being the substrate temperature and Q the activation energy for surface migration. The insensitivity of the growth rate to the substrate temperature is caused by two opposing tendencies. For classical CVD the T dependence of the surface migration increases the deposition rate, but in APIVT this is counteracted by the lower temperature difference between source and substrate (at constant source temperature), resulting in a lower arrival rate.

1.2.4 Ion assisted deposition

Ion assisted deposition (IAD) is based on electron-gun evaporation and subsequent partial ionization of silicon [40]. An applied voltage accelerates silicon ions towards the substrate. Typical acceleration voltages of 20 V are used. This yields the lowest etch-pit densities in monocrystalline epitaxial layers [41]. The principle of the IAD technique is shown in Figure 1.7.

Because of the energy supplied by the accelerated ions, the surface adatom mobility is enhanced. As a result the IAD technique enables epitaxial growth at temperatures as low as 435 °C with high deposition rates up to 0.5 μm/min. The Hall mobility of monocrystalline epitaxial

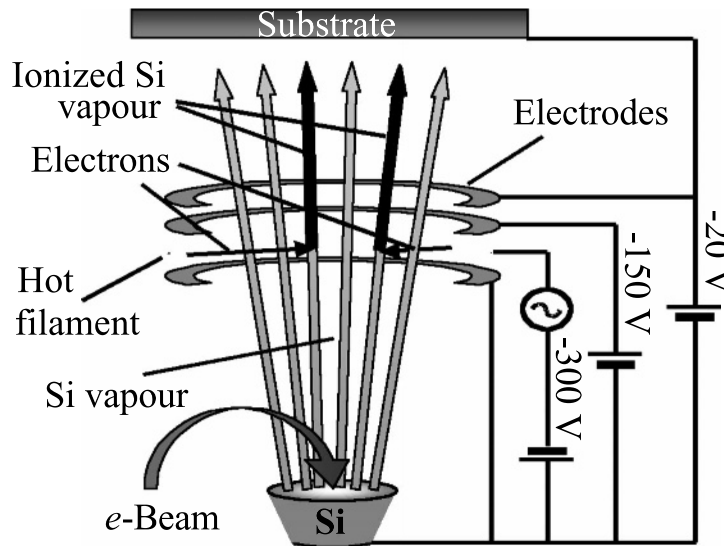

Figure 1.7 Schematic of the ion-assisted deposition technique [after 42].

layers increases with deposition temperature and reaches values comparable to those of bulk Si at $T > 540\,^{\circ}$C. The majority-carrier mobility in IAD boron-doped films almost reaches the theoretical values obtained for crystalline bulk silicon over the doping range 10^{16} to 10^{20} cm^{-3}. The electronic properties of the films are strongly dependent on the substrate orientation. In line with other findings valid for low-temperature epitaxial growth, the diffusion length is up to an order of magnitude lower in (111)-oriented Si films as compared to (100)-oriented Si films, resulting in inhomogeneous current collection in light-beam induced current measurements on epitaxial cells on multicrystalline Si substrates [43]. Photoluminescence and deep level transient spectroscopy revealed broad defect distributions for low deposition temperatures $<550\,^{\circ}$C. The point defect densities are up to four orders of magnitude lower in (100)-oriented Si epitaxial layers than in (111)-oriented Si films. Also temperature-dependent quantum efficiency (TQE) measurements were used to investigate the recombination behaviour in epitaxial silicon thin film solar cells grown by ion-assisted deposition [44]. The diffusion length in this material is dominated by Shockley–Read–Hall recombination via relatively shallow defects with activation energies of 70–110 and 160–210 meV, respectively. At a deposition temperature of 650– °C with a prebake at 810– °C [45], ion-assisted deposition produces epitaxial Si films with a minority-carrier diffusion length of 40 μm.

1.2.5 Low energy plasma enhanced chemical vapor deposition/electron cyclotron resonance chemical vapor deposition

Apart from accelerated ions, plasma techniques can also be used to provide additional energy to increase surface mobility and by doing so to allow high-quality epitaxial growth from a low-temperature deposition method.

Low energy plasma enhanced chemical vapor deposition is a technique in which a high current plasma discharge composed of low-energy particles leads to a high deposition rate,

while not damaging the wafer surface [46]. The main application for this technique is the growth of compositionally graded relaxed SiGe buffer layers for high-speed advanced metal-oxide-semiconductor (MOS) devices, but the technique is in principle also of great interest for solar cells.

An ECR source can also be used to provide a dense plasma that greatly enhances surface mobility and allows epitaxy at temperatures below 400 °C [47].

1.3 SILICON BASED EPITAXIAL LAYER STRUCTURES FOR INCREASED ABSORBANCE

Since crystalline Si is an indirect bandgap material, its absorption coefficient at wavelengths >900 nm becomes too small to absorb effectively incoming light at larger wavelengths in an epitaxial layer of only 20 μm. In order to increase the absorbance, one can modify the epitaxial layer by growing specific structures to increase the optical pathlength or through decreasing the bandgap by alloying with Ge.

1.3.1 Epitaxial growth on textured substrates

A first approach consists of chemically texturing the substrate before epitaxial growth. However, this approach also has drawbacks. The textured surface structure tends to flatten during the epitaxial process by facet formation, reducing the effectiveness of the texturing process. Moreover, due to the resulting surface roughness before epitaxy, the defect density in the epitaxial layer will be high and as a result it will be difficult to reach high open circuit voltage (V_{oc}) values.

The texturing can also be done by mechanical means, resulting in structures like the ones shown in Figure 1.8. The approach followed here is straightforward: by grooving the Si substrate

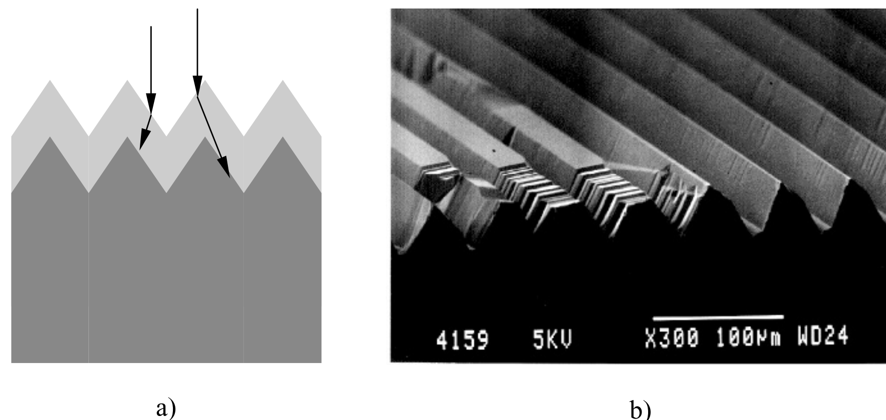

Figure 1.8 a) Schematic of the optical enhancement effect when grooving the substrate before the epitaxial growth assuming conformal growth; b) SEM picture illustrating the modification of the mechanically textured Si-surface after growth of an epitaxial layer when growing on a Si-substrate with different grain orientations.

before the epitaxial growth, the optical pathlength within the active layer is enhanced, as shown in Figure 1.8a when conformal growth is assumed. A minimization of the reflectance of the structure before and after grooving was studied [48]. When applying this technique to multicrystalline Si substrates one has to take into account the facetted growth of the epitaxial layer and the different growth rates on different crystallographic orientations. The consequence of this effect is illustrated in Figure 1.8b, showing the cross-section of an epitaxial layer grown on a mechanically textured surface. One can clearly observe the modified texture after epitaxial growth. On grains with orientations near (100) the texture is well preserved, whereas on other grain orientations the original texture has been modified by the development of different facets.

By means of this technique, large-area CVD-grown epitaxial cells ($100\,cm^2$) on UMG-Si were realized. Using an industrial solar cell process with screenprinted contacts, efficiencies between 12 and 13 % were obtained despite the limited thickness of the epitaxial layer which was between 15 and 20 μm [21, 49].

1.3.2 Silicon–Germanium alloys

A straightforward approach to increase the short circuit current is based on increasing the absorption coefficient of a crystalline Si by alloying it with Ge. The lower bandgap of the SiGe alloy allows the increase of the infrared absorption of the cell, although at the expense of a reduced solar cell open circuit voltage. In a bulk crystalline solar cell this loss will outweigh the gain in short circuit current. Solar cells realized in bulk $Si_{1-x}Ge_x$ substrates with x $<$ 10 % solar cells were reported [50], confirming the predicted behaviour. However, in thin film cells the reduction in open circuit voltage is, theoretically at least, less severe when surface recombination dominates over bulk recombination. By using a $Si/Si_{1-x}Ge_x$ heterojunction back surface field (BSF, see Figure 1.9a) most of the loss in open circuit voltage can theoretically be recovered. Figure 1.9b shows the typical cross-hatch pattern of a relaxed SiGe layer, epitaxially grown on a (100) Si substrate.

The experimental studies, conducted on relaxed $Si_{1-x}Ge_x$ epitaxial layers on Si for photovoltaic purposes were mostly restricted to alloys with Ge-content below 20 %, although theoretical calculations indicate there might be (limited) benefit from impact ionization at higher Ge-content [51, 52]. Thick relaxed $Si_{1-x}Ge_x$ layers with x ranging from 0 to 20 % were

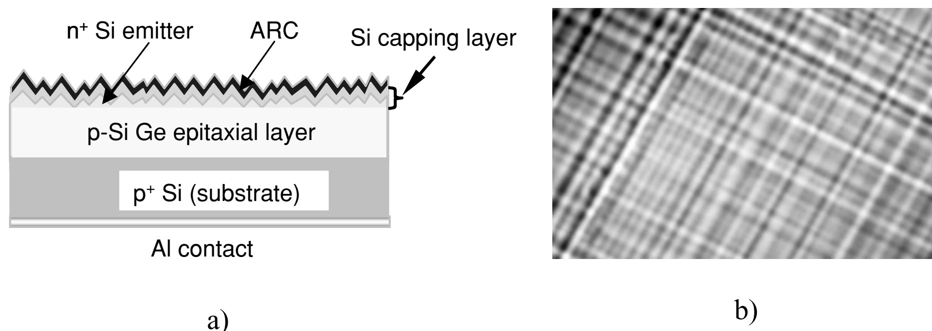

Figure 1.9 a) Basic structure of the SiGe thin film structure on Si; b) Optical micrograph of the typical cross-hatch pattern of a relaxed $Si_{.9}Ge_{.1}$-layer on Si; the magnification is 500x

grown epitaxially by CVD and LPE on highly doped monocrystalline Si substrates for solar cell purposes. Epitaxial SiGe alloys were grown by means of CVD in a lamp-heated system with graphite susceptor at reduced pressure (40 mTorr) and temperatures between 700 and 800 °C [53]. SiH_2Cl_2 and GeH_4 were used as Si and Ge precursors, respectively. Because of the relatively large thickness needed (in comparison with the strained layers needed for microelecronic applications), the growth rate should be as high as possible. Increasing the growth rate requires higher deposition temperature, but since the Ge-incorporation efficiency decreases at higher temperatures, a trade-off has to be looked for. This can be seen in Figure 1.10. As a

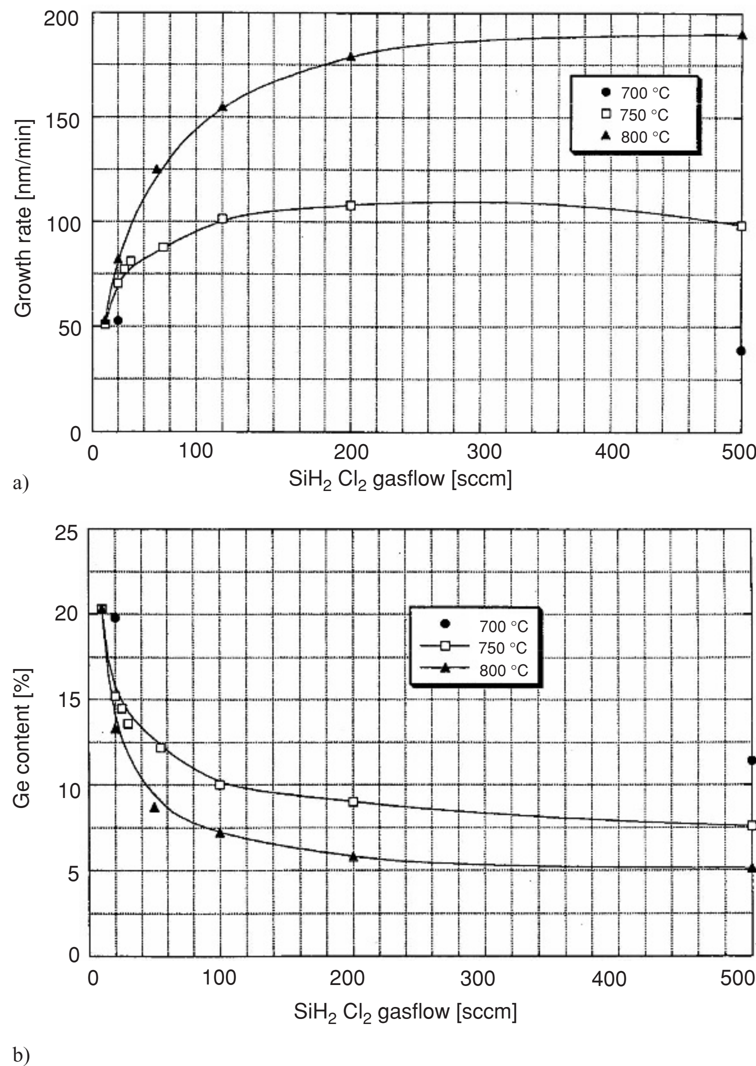

Figure 1.10 a) Growth rate of the epitaxial $Si_{1-x}Ge_x$-layers as a function of the mass flow of SiH_2Cl_2 (the 1 %GeH_4 in H_2 flow was kept constant at 200 sccm); b) Ge-incorporation a.f.o. SiH_2Cl_2 gasflow for different temperatures (the GeH_4/H_2 flow was the same as for a.)

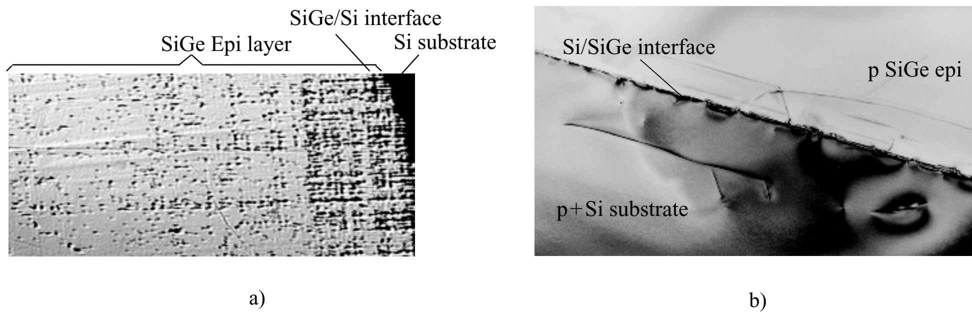

Figure 1.11 a) Defect density a.f.o. depth as revealed by optical analysis of beveled relaxed $Si_{.9}Ge_{.1}$-layers on Si; b) Cross-section TEM picture of dislocations confined within the buffer layer of the same structure as in Figure 1.11a. One can observe the bending of the dislocation lines within the buffer layer.

result, growth rates between 0.15 and 0.2 μm/min were obtained for the layers studied within the solar cells.

Because of the lattice mismatch between the $Si_{1-x}Ge_x$-layer and the Si-substrate it is necessary to incorporate a buffer layer in between the Si substrate and the active layer. When the $Si_{1-x}Ge_x$-thickness (10–15 μm) greatly exceeds the critical thickness [54] for growth on Si (which will always be the case), misfit dislocations relax the lattice strain, resulting from the lattice mismatch.[6] The density of dislocations throughout a bevelled epitaxial $Si_{1-x}Ge_x$-layer on Si can be seen in Figure 1.11a. When grown under suitable conditions and at sufficiently high temperature, the misfit dislocations will partially annihilate within the buffer layer. On bevelled samples which were subjected to a defect etch, the evolution of the defect density as a function of depth was determined. This is shown in Figure 1.11a where a strong reduction of the dislocation density towards the upper surface is clearly seen. The defect density decreases from 10^7 cm^{-2} in the buffer to 10^5 cm^{-2} at the top surface of the layer. The confinement of the misfit dislocations was also verified by cross-section transmission electron microscopy (TEM) (see Figure 1.11b).

By means of EBIC measurements on Schottky diodes on the as-deposited relaxed $Si_{1-x}Ge_x$-layers, the diffusion length was extracted [55]. Despite the defect density being in the order of 10^5 cm^{-2} an effective diffusion length of 80 to more than 100 μm was extracted for CVD layers as well as for LPE layers when a buffer layer was used. The term effective diffusion length is used because the layer thickness is only 20 μm thick. It also proves that, at room temperature at least, the dislocations in a CVD-grown layer are not necessarily more active than in LPE-grown layers.

Solar cells were processed in these relaxed $Si_{1-x}Ge_x$-layers on p^+-Si by a laboratory process comprising solid source diffusion, nitride surface passivation and evaporated contacts, the details of which can be found in [56]. The short circuit current observed for the cells with a relaxed $Si_{1-x}Ge_x$ layer was higher than for a Si thin film crystalline Si solar cell with comparable active layer thickness and similar doping profile, but the enhancement of the short circuit current saturates at Ge-content larger than 10 %. However, open circuit voltage and

[6] The difference in lattice constant between Si and Ge is about 4 %. The lattice constant of the SiGe alloy varies practically in a linear fashion between the lattice constant of Si and Ge (Vegard's law).

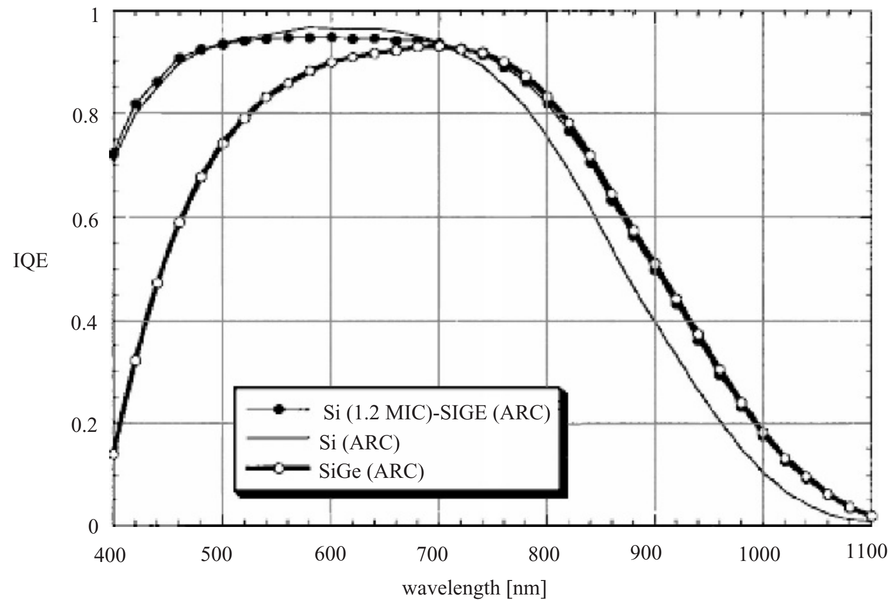

Figure 1.12 IQE-curve of epitaxial solar cell with relaxed SiGe-base ([Ge] = 10 %) and comparison with response of an epitaxial Si solar cell with equal active layer thickness. Reproduced figure 10 with permission from K. Said, J. Poortmans, M. Caymax, J. F Nijs, L. Debarge, E. Christoffel, A. Slaoui, 'Design, fabrication, and analysis of crystalline Si-SiGe heterostructure thin-film solar cells', IEEE Trans. El. Dev. Vol.46, no:10; Oct.1999; p.2103–10. Copyright (1999) IEEE.

fill factor were substantially lower than for the Si reference cell. One of the important items when using $Si_{1-x}Ge_x$-alloys is the surface passivation. Although the use of plasma enhanced chemical vapor deposition (PECVD)-nitride passivates the front surface to some degree, the blue response of the cell is significantly lower than for a Si reference cell. The blue response is improved by the use of a Si capping layer on top of the structure. The positioning of the Si–$Si_{1-x}Ge_x$ transition relative to the junction is very important to avoid excessive recombination near the interface between the Si capping layer in which the emitter is diffused and the $Si_{1-x}Ge_x$ base layer. The Si on top relaxes in its turn resulting in a defect density in the Si layer of the order of 10^7 cm^{-2}. The internal quantum efficiency (IQE) curve in Figure 1.12 shows the effect of enhanced red response in the base resulting from the alloying with Ge and the improved blue response by the use of an optimized Si capping layer. But even under these circumstances the voltage penalty is too high to get an improved efficiency as compared to the thin film crystalline Si reference cell, as can be seen from Table 1.1.

1.3.3 Germanium–Silicon structures

In order to avoid crystallographic defect formation occurring upon relaxation of a SiGe layer with a thickness larger than the critical thickness, other approaches have been proposed and tested recently. One approach consists in growing Ge layers embedded in a Si matrix by forming three-dimensional islands in the Stranski–Krastanov growth mode. The embedded Ge layers

Table 1.1 AM1.5 illuminated I-V-characteristics of a thin film epitaxial $Si_{.9}Ge_{.1}$ solar cell on a p^{+}-Si substrate in comparison to thin film crystalline Si solar cell on the same substrate. The active layer thickness was 15 μm with a Si capping layer of 1 μm

Active layer material	Short circuit current [mA cm^{-2}]	Open circuit voltage [mV]	Fill factor [%]	Efficiency [%]
$Si_{.9}Ge_{.1}$	28.8	575	77.5	12.8
Si	27.9	634	79.2	14.0

increase the infrared absorption in the base of the cell to achieve higher overall photocurrent and to overcome the loss in open circuit voltage of the heterostructure. Usami *et al.* [57] report on the performance of solar cells with stacked self-assembled Ge dots in the intrinsic region of Si-based p-i-n diode. These dots were epitaxially grown on p-type Si(100) substrate via the Stranski–Krastanov growth mode by gas-source molecular beam epitaxy. The layer stack is shown in Figure 1.13a.

An enhanced external quantum efficiency (EQE) in the infrared region up to 1.45 μm was observed for solar cells with stacked self-assembled Ge dots compared with the structure without Ge dots, as can be seen from Figure 1.13b. Furthermore, the EQE was found to increase with increasing number of stacked layers. Similar work was reported by Presting *et al.* [58]. In an ultra high vacuum molecular beam epitaxy (UHV-MBE) chamber up to 75 layers of Ge, each about eight monolayers thick, separated by Si-spacer layers (9–16 nm) were grown on each other using standard 10 Ω-cm p-type Si-substrates. The density of islands in the layers was increased by the use of antimony as surfactant resulting in densities $>10^{11} cm^{-2}$. The islands were covered by a 200 nm thick Si-layer (n-type) on top which is used as the emitter of

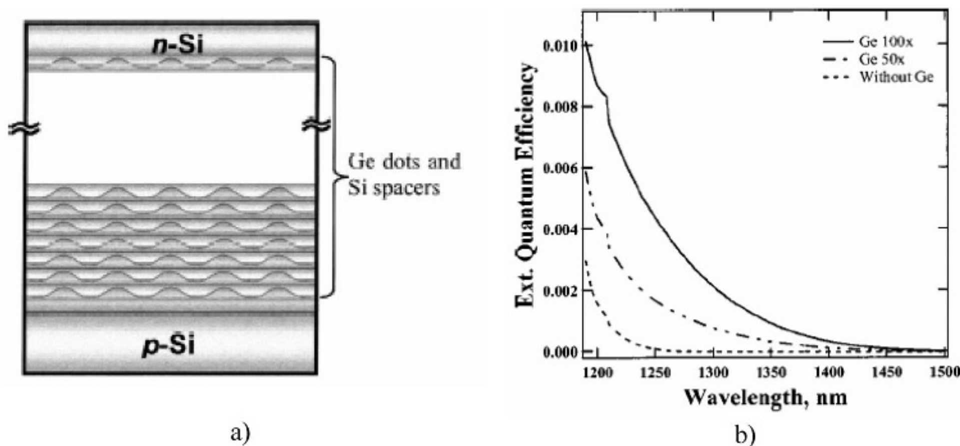

Figure 1.13 a) Cross-section of the Si-Ge layer structure grown in [57]; b) spectral photocurrent extracted from the structure in [57]; Reused with permission from Arnold Alguno, Applied Physics Letters, 83, 1258 (2003). Copyright 2003, American Institute of Physics.

the cell. Photocurrent measurements confirmed the higher response of the fabricated solar cells in the infrared region compared to standard Si-cells. It remains unclear whether the voltage penalty can be overcome by this approach.

For the sake of completeness, it has to be noted that, within the frame of space solar cells, the growth of GaAs layers on a Si-carrier has received a lot of attention. Very often, a Ge template layer is grown between the Si substrate and GaAs active layer to accommodate the lattice mismatch between Si and GaAs [59, 60]. The discussion of these advanced approaches goes beyond the scope of this chapter.

1.3.4 Epitaxial layers on a buried backside reflector

Despite the clear experimental evidence of enhanced photocurrents, no group has been able to prove experimentally that the current increase from including a $Si_{1-x}Ge_x$ alloy or embedded Ge layers in the active layer structure of the solar cell is sufficient to overcome the voltage penalty. As a result the photocurrent increase does not result in an enhanced efficiency as compared to Si solar cells with equal active layer thickness. Therefore substantial effort is being put into developing material systems which allow reflection at the interface between the Si substrate and the Si epitaxial layer and thereby allow optical confinement. Reflection can only occur by having a medium with a different refractive index in between the Si substrate and the epitaxial layer. The main restriction within the context of this chapter is that this medium should allow epitaxial growth. Grossly speaking, one can distinguish two basic solutions, which are shown in Figure 1.14. The first one is based on the use of a porous Si interlayer. By means of the porosity one can control the refractive index while at the same time the porous Si acts a template for epitaxial growth by retaining the crystallographic information of the substrate beneath (at least when the porous Si is formed by anodization in an HF-containing solution). The second solution relies on epitaxial overgrowth over a dielectric or metallic layer with windows allowing a crystallographic connection to the Si substrate.

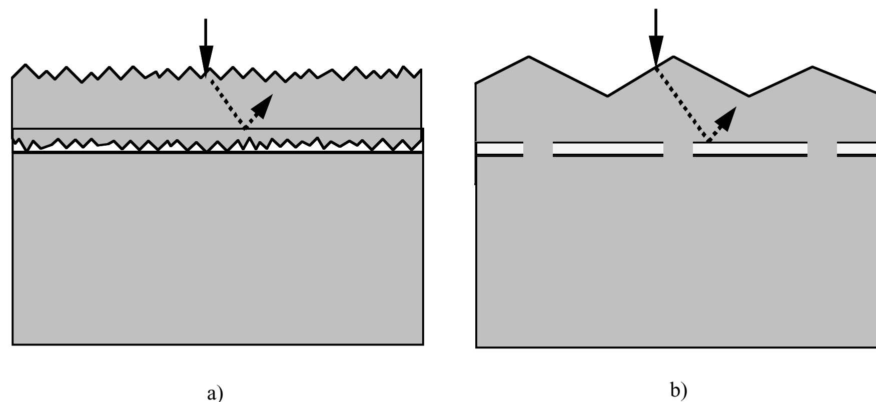

Figure 1.14 a) Schematic of porous Si interlayer approach; b) Schematic illustration of lateral epitaxial overgrowth approach

1.3.4.1 Epitaxial layers on buried porous Si interlayers

Electrochemical etching of porous silicon is an excellent technique to create multiple Bragg reflectors that can be used, for instance, in optical cavities. The refractive index of the different layers of the Bragg reflector are controlled by the porosity, which is determined by the anodization conditions (current density, HF-concentration in the solution). As porous silicon retains the crystallographic information of the original crystal it is etched into, the application of a silicon deposition process can lead to ordered deposition defined by the original crystal structure of the substrate. It therefore seems ideal for the purpose described above [61, 62].

Significant efforts have been made to model and optimize the reflectance of the porous Si interlayer. Zettner *et al.* [61] and Abouelsaood *et al*. developed a model for light propagation in porous silicon (PS) based on the theory of wave propagation in random media [63]. The modeling in the latter is based on silicon being the host material in combination with randomly distributed spherical voids as scattering particles. The specular and the diffuse part of the light scattering were determined and treated separately.

The challenge in the experimental implementation of this concept is to maintain the reflector properties during the silicon deposition process, which often takes place at high temperature, where porous silicon is not stable. Porous silicon tends to reorganize itself towards a low energy configuration with larger, spherical voids. Moreover, a phenomenon of pore filling can occur: some of the deposited silicon enters and gets incorporated in the porous structure, lowering the porosity. Two approaches can be followed. One can attempt to preserve the porous silicon structure as much as possible by carrying out the deposition at low temperature, for instance with LEPECVD [64]. This technique allows one to deposit a Si film with an epitaxial quality on the top of PS without destroying its multilayer structure (as revealed by high-resolution X-ray diffraction and cross-sectional transmission electron microscopy shown in Figure 1.15a). The epilayers of 10 μm are grown at very high deposition rate (around 3 nm/s) at 590 °C. TEM-analysis reveals that during the deposition a high density of defects forms at the interface PS/epi-Si and spreads through the whole epilayer. The defect density is decreased when the deposition temperature is increased to 645 °C. The second approach is to carry out epitaxy at high temperature, and live with the reorganization that will inevitably occur. Remarkable

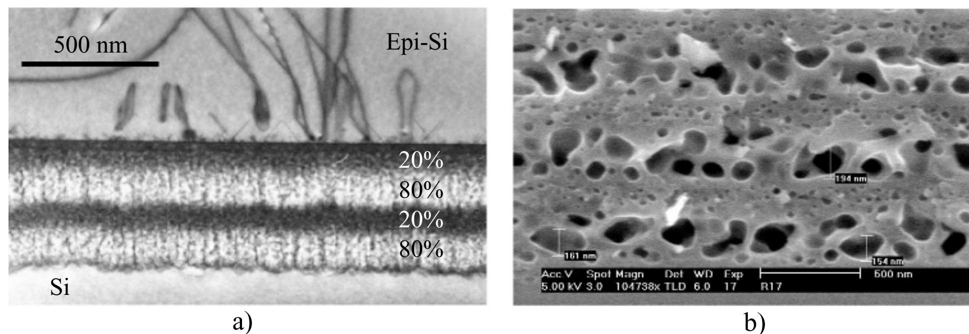

Figure 1.15 Buried porous silicon reflectors: a) TEM-picture of epitaxial layer grown on top of a porous Si layer structure at low temperature; b) SEM micrograph of an annealed porous Si reflector consisting of multiple high-porosity/low-porosity bi-layers. The porous layer was subjected to an annealing at T = 1150 °C.

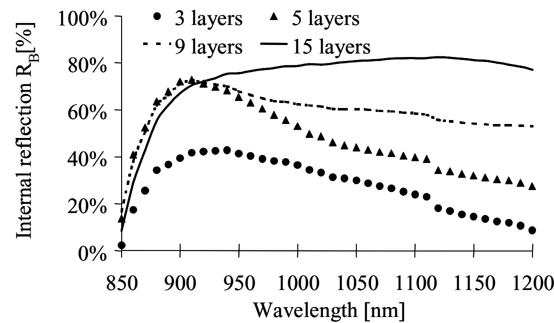

Figure 1.16 Curves of the back reflectance derived from reflectance measurements, achieved with differerent PS reflectors (from reference [[67]).

results with this approach were recently reported [65]. Porous silicon multilayers consisting of several low-porosity/high-porosity stacks were formed by electrochemical etching on highly p-doped single crystalline silicon. The samples were then brought to high temperature and underwent an epitaxial deposition process with thermal CVD. A scanning electron microscopy (SEM) micrograph of the structure in Figure 1.15b clearly shows that the porous silicon, with original pore size in the order of a few nanometers, has completely reorganized into layers with large voids and wide pore walls. The overall structure with alternating high/low porosities is, however, maintained. Strikingly, the structure after reorganization appears to function rather well as a Bragg mirror. This can be seen in Figure 1.16, where the internal back reflectance (R_B) at the porous silicon/epitaxial layer interface, as calculated from the samples' total reflectance, is plotted as a function of the wavelength. The internal reflectance increases with the number of porous silicon layers and reaches a top value around 80 % for a stack of 15 layers in a broad wavelength range. Resistance measurements show that this type of buried reflector does not significantly hinder the vertical flow of majority carriers. It therefore shows great promise for high current epitaxial solar cells.

Liquid phase epitaxy has also been studied for growing Si epitaxial layers on porous Si. In [66] the porous silicon formation by HF anodization on (100) or (111) Si wafers is realized in the first step, followed by annealing in an H_2 atmosphere, and finally LPE silicon growth was made with different temperature profiles in order to obtain a silicon layer on the sacrificial porous silicon (p-Si). Pyramidal growth was found on the surface of the (100) porous silicon but the coalescence was difficult to obtain. However, on a p-Si(111) oriented wafer, homogeneous layers were obtained.

Besides acting as a template for epitaxial growth, the porous Si buried layer can also act as a gettering layer to prevent contaminants from diffusing from the Si carrier substrate into the active epitaxial layer. The principle of using porous-silicon-gettered MG-Si as a low cost epitaxial substrate for polycrystalline silicon thin film growth for solar cells has been proven by Tsuo *et al.* [67].

1.3.4.2 Epitaxial lateral overgrowth

Epitaxial lateral overgrowth (see Figure 1.14b) is a well known technique which is often based on selective epitaxial growth of Si through openings in a dielectricum. The dielectricum

most often studied as a masking layer is thermal oxide. Selectivity in CVD is obtained by controlling the balance between Si etching and growth in a Cl-containing atmosphere. In order to overgrow the dielectricum, the lateral growth rate is preferentially enhanced as compared to the vertical growth rate. As this is a difficult task, the only way to obtain closed Si layers over the dielectricum is to keep the distance between the openings approximately two times the desired layer thickness.

Because of its close-to-equilibrium character, it is most often easier to grow with a selectively high horizontal to vertical growth by means of LPE. The growth is mostly done on (111) Si substrates as this allows the growth of smooth layers [68] (see Figure 1.17a), although the *in situ* texturing during LPE-growth on (100) Si substrates would be a valuable asset. An interesting variation on this theme is the creation of a buried reflector by means of electrodeposition. The proof-of-concept was done on patterned, metal-masked silicon substrates by a liquid-phase electro-epitaxial lateral overgrowth process [69] (see Figure 1.17b). Silicon films were grown from liquid metal solutions (molten bismuth saturated with silicon) by current-induced crystallization on stripe-patterned, W-masked (111) silicon substrates. Tungsten was chosen because it resists the high temperatures during the electrodeposition and is not chemically attacked by the molten metal. Growth temperatures range from 800 to 1150 °C, and a current density of 2–20 A/cm^2 was imposed across the silicon/melt interface to enhance the lateral growth. Continuous (over 1 cm^2 areas) epitaxial layers of silicon were achieved on W-masked substrates patterned with 10 μm wide stripe openings spaced 100 μm apart.

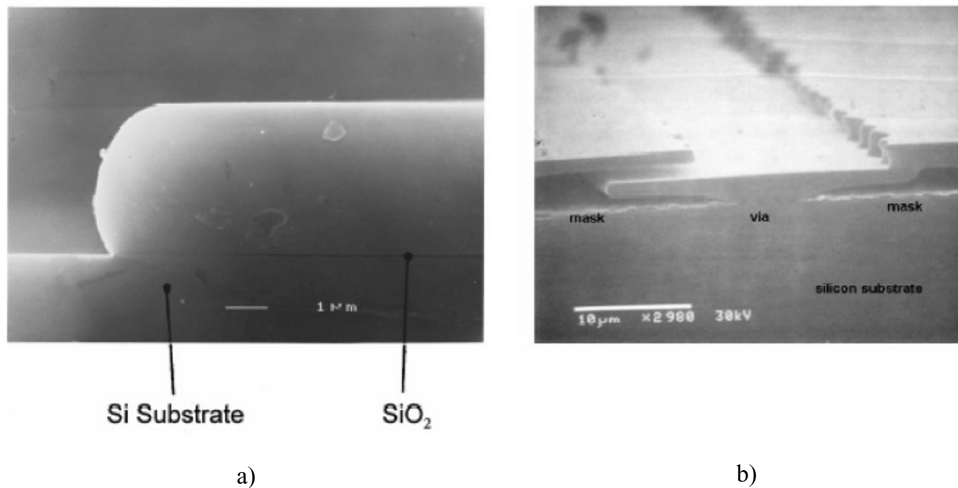

Figure 1.17 a) Epitaxial lateral overgrowth by means of LPE through openings in a dielectricum layer on top of a (111) Si substrate. The experimental aspect layer width/layer height ratio is 43, the picture was taken from ref. [68]; Reused with permission from H. Raidt, Journal of Applied Physics, 80, 4101 (1996). Copyright 1996, American Institute of Physics.; b) Illustration of the electro-epitaxial lateral overgrowth over a tungsten buried reflector (taken from ref. [69]). Silicon is growing from the stripe opening in mask. The right side has been connected with the silicon overlayer seeded at the adjacent via, but the left side is misaligned and interleaved with silicon at adjacent via. Reproduced with permission from *Journal of Crystal Growth,* **225**, M. G. Mauk and J. P. Curran, Electro-epitaxial lateral overgrowth of silicon from liquid-metal solutions', pp. 348–353. Copyright (2001) Elsevier.

1.4 EPITAXIAL SOLAR CELL RESULTS AND ANALYSIS

1.4.1 Laboratory type epitaxial solar cells

Although the substrates of interest for epitaxial solar cells are low cost Si substrates, substantial work has been reported on reference mono- and multicrystalline Si substrates. Epitaxial cells on highly doped monocrystalline Si substrates were reported by several groups in the early nineties to demonstrate the efficiency potential of the epitaxial solar cell approach (see e.g. references [70] for CVD-grown cells and [71, 72] for LPE-grown Si layers). Table 1.2 provides an overview of the best efficiency results obtained in epitaxial layers grown by various techniques and processed according to different *laboratory* solar cell process schemes. The experimental results obtained on monocrystalline highly doped substrates confirm the large efficiency potential of thin film crystalline Si solar cells, especially when combined with a suitable backside reflector (the intermediate oxide layer in case of the silicon-on-insulator by implantation of oxygen (SIMOX substrate or by etching back the Si substrate to improve the optical confinement properties of the structure). Some reports provide an indication that crystallographic defects in the epitaxial layer are created by the lattice mismatch which exists between the highly doped Si substrate and the epitaxial layer. This lattice mismatch is small but in view of the large thickness of the epitaxial layer, strain relaxation occurs through the introduction of misfit dislocations [73].

When epitaxial growth by means of CVD is performed on highly doped multicrystalline substrates (ribbons, MG-Si, p^+-multicrystalline Si), the efficiencies of laboratory type cells are clearly lower as compared to the demonstration epitaxial cells on monocrystalline Si substrates.

Table 1.2 Overview of main results on laboratory type epitaxial cells

Growth technique	Type of substrate	Thickness [μm]	Cell area [cm^2]	Solar cell process	Efficiency [%]
CVD-grown epitaxial layers					
CVD	Mono (SIMOX)	46	4	High-efficiency interdigitated process Evaporated contacts	19.2 [8]
CVD	p^+-Mono	37	4	ISE high-efficiency process	17.6 [78, 79]
CVD	p^+–SILSO	20	4	Homogeneous etched-back emitter Evaporated contacts	13.8 [49]
CVD	p^+-EFG	20	4	Homogeneous etched-back emitter Evaporated contacts	13.2 [49]
LPE-grown epitaxial layers					
LPE	p^+-mono	35	4	Evaporated contacts + back-etch of substrate	18.1 [80]
LPE	p^+-mono	30	4	Evaporated contacts (drift-field in epitaxial layer)	16.4 [76]
LPE	p^+-multi				15.4 [77]

A process step during which H is introduced in the epitaxial layer, either by remote plasma hydrogenation or a firing-through-nitride step has been proven to be crucial to passivate the defects in the epitaxial layers [18, 21, 48, 49]. This has allowed solar cell efficiencies near to 14 % in epitaxial layers of only 20 μm for small-area cells.

Solar cells fabricated on LPE-grown epitaxial layers display open circuit voltages above 660 mV (air mass number (AM) l.5, 25 °C) [74], confirming the high electronic quality of the epitaxial layer. As a result, the best solar cells made in LPE-grown layers have efficiencies in the range 17–18 % [75]. An important step in obtaining these high cell efficiencies is the removal of most of the heavily doped substrate on which the epitaxial layer is grown to boost the backside reflectance. In this way the cell efficiency can be increased by nearly 25 % when the cell is thinned to a thickness of 30 μm. As mentioned earlier, LPE allows the incorporation of a doping profile in a straightforward fashion into the epitaxial layer. In reference [76] a Ga doping gradient was intentionally introduced throughout the film to produce a drift field in the base of the solar cell, thus enhancing the effective minority-carrier diffusion length and increasing the long-wavelength response. An independently confirmed efficiency of 16.4 % was achieved on an LPE drift-field thin film silicon solar cell.

The efficiency potential has been further confirmed by small-area LPE-grown epitaxial cells on multicrystalline Si substrates. Such cells have displayed efficiencies up to 15.4 % [77].

1.4.2 Industrial epitaxial solar cells

Within the context of this chapter, 'industrial solar cell' is equivalent to large-area solar cell ($>20\,cm^2$), made by a production process which is similar to the practices in the PV industry. Although the generic process flow to produce a solar cell in an Si epitaxial layer is very similar to the cell process for a classical Si solar cell, the subject deserves to be treated within a separate chapter for two reasons. First of all, making large-area cells is an indication of the maturity of a certain epitaxial deposition technology (homogeneity in thickness and doping over a larger area). Second by, despite the generic resemblance to the solar cell process, steps like front surface texturing have to be tuned for epitaxial cells. In the latter it does not make sense to use the texturing techniques widely used for bulk crystalline Si solar cells as these techniques would remove most of the epitaxial layer; typically, the texturing step removes 10–20 μm of Si.

The main reported results are summarized in Table 1.3. Efficiencies up to nearly 14 % on Czochralski-silicon (Cz-Si) and 13 % on highly doped multicrystalline Si substrates have been achieved by applying an industrial process scheme based on tube or in-line P diffusion, as well as screen-printed front and back contacts fired through a SiN_x anti-reflection coating [81, 82]. Light-beam induced current measurements show that the diffusion length distribution is quite inhomogeneous over the whole cell area. A maximum effective diffusion length of about 25 μm and mean values around 15 μm were found in typical epitaxial solar cells [83]. Characterization of the solar cells by infrared lock-in thermography revealed local shunts as shown in Figure 1.18. In some circumstances these local shunts were correlated with well defined epitaxial defects [84].

To reduce the front surface reflectance and enhance the optical path length, the front surface of the epitaxial cell should be textured. This is a common step in most industrial processes for bulk crystalline Si solar cells, but the process has to be adapted for epitaxial solar cells. The most crucial element is to minimize the amount of silicon removal to keep the starting thickness of the epitaxal layer as low as possible. One process, already used in industrial solar

Table 1.3 Main efficiency results obtained on epitaxial solar cells produced by industrial process flows

Growth technique	Type of substrate	Thickness [μm]	Cell area [cm^2]	Solar cell process	Efficiency [%]
CVD	p$^+$-Cz-Si (reclaimed)				13.8[81]
CVD	p$^+$-SILSO	20	25	Screenprinting (firing through nitride)	12.5 [21]
	Epitaxial layer on grooved p$^+$-SILSO	20	25	Screenprinting (firing through nitride)	13.2 [21]
	p$^+$-SILSO	40	20	Laser-grooved buried grid technology	11.9 [21]
CVD	UMG-Si	25	20	Screenprinting (firing through nitride)	12.9[82]
		100	20	Screenprinting (firing through nitride)	12.2[82]
LPE	UMG-Si (melt-back method)	Small area	30	Phosphorus diffusion from pastes	10[86]

cell fabrication to texture multicrystalline silicon solar cells, is based on chemical isotexturing. This wet chemical etching based on HF and HNO_3 starts on the defects of the saw damaged surface, and creates a textured surface with etch pits of 1 to 10 μm in diameter. However, on epitaxially grown layers, this process does not start uniformly because the surface is essentially damage free. Instead of obtaining a homogeneously textured surface, deep holes are formed on the surface at defects in the epitaxial layer. Therefore, a new plasma texturing technique was developed based on SF_6 chemistry and plasma generation with microwave antennas and specifically tuned for epitaxial solar cells. In particular, the amount of Si removal was minimized while keeping the reflectance low. This texturing process removes only 2 μm of the epitaxial

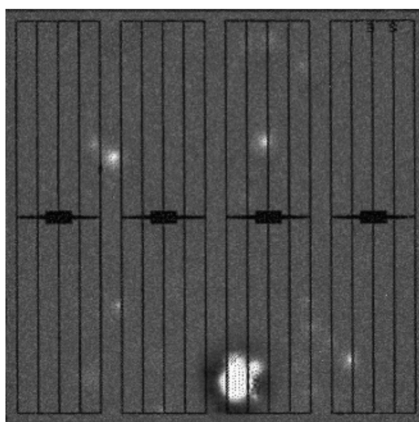

Figure 1.18 Picture showing local shunting paths as revealed by IR-thermography . The fingerstructure is shown in overlay (courtesy of FhG-ISE, Freiburg, Germany).

layer. With this process, efficiencies near 13 % were obtained in CVD-grown epitaxial layers on UMG-Si substrates.

The first modules based on epitaxial solar cells, grown on highly doped monocrystalline or multicrystalline Si substrates, were recently reported [85]. The module based on monocrystalline substrates showed an efficiency of 12.2 % (cell aperture area was 368 cm^2), whereas the one based on multicrystalline Si gave an efficiency of 10.2 % (the aperture area in this case was 576 cm^2). Both results give evidence of the fastly progressing maturity of this solar cell technology.

Industrial type solar cells have also been realized on LPE-grown layers. In comparison with CVD-grown epitaxial layers where the difference between industrial and laboratory type solar cell efficiencies is in the range of 1 % (for layers grown on highly doped multicrystalline Si substrates), the efficiency gap is much larger between laboratory type and industrial LPE solar cells. This is caused by the difficulty in obtaining LPE-layers with uniform topology over the whole area. Solar cells, fabricated by a P paste diffusion, have shown efficiencies up to 10.0 % [86].

1.4.3 Special epitaxial solar cell structures

Front grid contacted thin epitaxial silicon solar cells based on the growth of crystalline silicon films on a substrate or superstrate have been reported for many years, as have wafer based solar cells with alternative contact approaches. Integrating these two concepts into a single device presents an opportunity for simultaneously reducing two major loss mechanisms associated with crystalline silicon solar cells. A proof-of-concept thin epitaxial silicon solar cell with an embedded semiconductor grid as an alternative to a conventional front metallic grid was developed by Aiken *et al.* [87] by means of lateral epitaxial overgrowth (see Figure 1.19). It resulted in a thin epitaxial silicon solar cell with a 7.8 % designated area conversion efficiency, well isolated contacts, negligible series resistive power loss, and less than 1 % shading of the designated area.

1.5 HIGH THROUGHPUT SILICON DEPOSITION

Despite its generic resemblance to a classical bulk crystalline Si solar cell process, the development of a manufacturing technology based on epitaxial solar cells requires two additional issues to be solved. The first is related to the commercial availability of a low cost Si substrate.

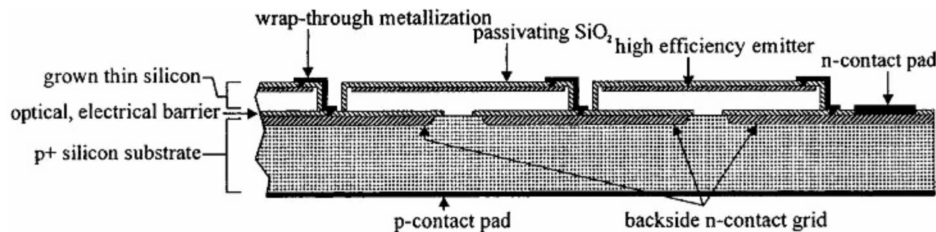

Figure 1.19 Schematic of the novel epitaxial cell structure as developed by Aiken *et al*.

As shown in the previous chapters there is ample evidence that efficiencies near 14–15 % are achievable in the short term with an epitaxial cell process using MG-Si substrates. The availability is mainly a matter of upscaling the infrastructure to produce this feedstock material as well as finding companies willing to crystallize this material to produce large multicrystalline Si ingots and to wafer them.

The second issue concerns the development of high throughput deposition equipment to grow epitaxial layers at a rate of several m^2/h for epitaxial layer thicknesses between 5 and 20 μm. This throughput is definitely higher than typically reached in commercial epitaxial reactors as developed for the microelectronic sector, which are rather aimed at obtaining a very high uniformity of thickness and doping (in the order of 1 %). The same upscaling challenge exists obviously for other thin film technologies based on a-Si:H or μc-Si:H layers, but in the case of epitaxial cells, the technical difficulties to be solved are considerable. In order to achieve high growth rate in the order of a μm/min and high crystallographic quality the temperature range of interest is between 800 °C and 1300 °C, which requires the use of materials withstanding high temperatures. Despite the high temperature prevailing during deposition, contamination of the crystalline Si layer during growth has to be prevented, putting stringent requirements on the purity of the used materials. But both in CVD and LPE one is confronted with potentially corrosive and aggressive gases or liquids. Finally there are conflicting requirements concerning the chemical efficiency[7] of the Si deposition process and the thickness uniformity. A high uniformity normally does not go along with a high efficiency since the latter points to a depletion in the gas phase. Even taking into account that the uniformity requirement for thickness and doping is in the order of 10 %, it remains a considerable issue.

Even when these problems are satisfactorily solved, the reliability and safety of the developed deposition equipment over time as well as its low cost-of-ownership will have to be proven. The allowable cost comprising the depreciation of the investment cost, and the cost of consumables (gases, susceptors, . . .) and maintenance depends obviously on the efficiency reached, but in order to be compatible with 1 € /W_p this should not be higher than 20 € /m^2, assuming a module efficiency of 14 % [15].

Clearly, presently one has not yet reached this point. Rather one sees presently a number of emerging high throughput deposition reactor concepts to tackle the main challenges. These concepts are aimed essentially at upscaling the CVD and LPE methods and will be discussed in the next sections. It should not come as a surprise that the upscaling efforts are mainly focusing on CVD and LPE giving their relative maturity versus other solutions like IAD. It is expected that the build-up of sufficient confidence in these reactor concepts will still require a number of years before one can foresee their integration into existing solar cell production lines.

1.5.1 Chemical vapor deposition reactor upscaling

1.5.1.1 Continuous chemical vapor deposition reactor

The first reactor concept comes closest to the in-line solar cell processing concept which one encounters in most present production facilities for bulk crystalline Si solar cells. It is

[7] Chemical efficiency is defined as the ratio of the Si which ends up in the active layer versus the amount of Si introduced in the gaseous or solid phase.

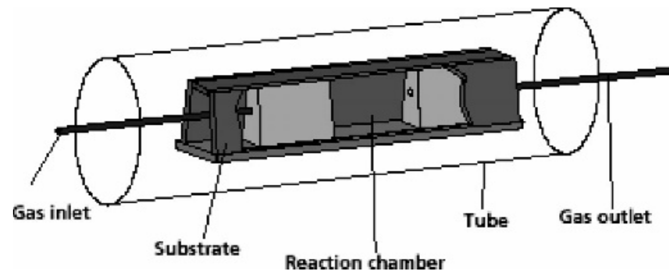

Figure 1.20 Schematic view on the tube-in-tube concept for the continuous CVD system developed at FhG-ISE, Freiburg; courtesy of FhG-ISE, Freiburg.

essentially based on continuous transport of the wafers through the hot reaction zone where the epitaxial deposition takes place. In order to achieve a high conversion efficiency ($Si_{(g)} \longrightarrow Si_{(s)}$) with only minor parasitic depositions, this reactor concept relies on a tube-in-tube concept [88, 89]. The rectangular substrates form the side walls of the reaction chamber (the inner tube) and constitute the largest part of its inner surface. The chamber is placed within the outer tube, flooded by H_2 or inert gas. The reactive gases, a mixture of $SiHCl_3$ (TCS) and H_2, are fed into the chamber and deposition occurs. In the continuous CVD (Con-CVD) reactor two rows of substrates slide continuously along the chamber, as shown in Figure 1.20. This also solves the problem of lateral uniformity and gas depletion as all substrates pass through the same reaction profile. To prevent, or at least reduce, the outdiffusion of reactive gases from the chamber into the outer tube, a small overpressure is maintained.

A gas curtain system ensures the separation between the inner atmosphere in the reaction zone and the outer atmosphere. This allows the substrates to be fed into and out of the reactor in a continuous way without gas exchange between reactor and laboratory. It is based on the behaviour of a gas diffusing against the flow of another gas. A small flow in the order of some cm/s reduces the concentration of the diffusing gas after a few centimetres against the flow direction to negligible values. Figure 1.21 shows the principle of the gas curtain systems which are installed at both ends of the reactor tube.

FhG-ISE has built the first test reactors using this concept [88, 89]. The most important features of the ConCVD reactor are shown in Figure 1.22.

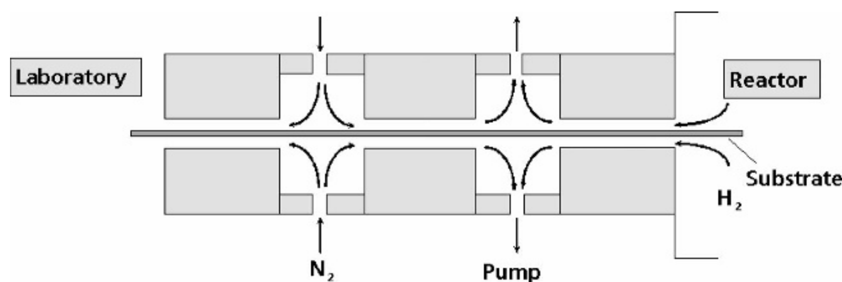

Figure 1.21 Gas curtain system to separate inner reactor atmosphere from outer atmosphere in the continuous CVD apparatus. See also [89].

a)

Open system with gas curtains and two rows of continuously moving substrates

Substrate temperature up to 1300 °C, resistively heated

Reactor tube SiC, 30 cm Ø

Reaction chamber: graphite, 40 cm long

Two rows of graphite carriers for the substrates: substrate width 10 or 20 cm, substrate length up to 40 cm; substrates of 10 cm width are placed in two rows one upon the other on each carrier

Gas lines into the reaction chamber for H_2, $SiHCl_3$ and B_2H_6, for H_2 or inert gas into the tube

Production rate at 5µm/min average deposition rate: 1.4 m_/h for Si layers of 30 µm thickness

b)

Figure 1.22 a) View on the ConCVD apparatus available at FhG-ISE, Freiburg; b) Summary of the main features of the present ConCVD-reactor.

Using this reactor, epitaxial layers were grown at 1150 °C on highly doped multicrystalline Si substrates at a deposition rate of about 1.5 µm/min and a throughput of 1.2 m^2/h. Using a relatively simple solar cell process, an efficiency of 12.5 % was reported [90].

First cost estimations have been made for this type of reactor. A production type ConCVD system featuring a 2m long reaction chamber (instead of the present 0.4 m) at 200 mm width would have a throughput of 150 000 m^2/year which in the end results in an estimated cost for silicon epitaxy of around 10 € /m^2, which is compatible with the cost goal stated before. The major cost share is H_2 consumption, which can be further decreased by application of state-of-the-art H_2 recycling [88].

1.5.1.2 Convection assisted chemical vapor deposition

Convection assisted CVD (COCVD) is a recent development which actively uses thermal convection to control the gas flow inside the reactor and to implement, in a natural manner, recycling of the nonused gaseous precursor. The concept of COCVD is shown in Figure 1.23 [91]. The reactor is tilted by an angle α against the horizontal orientation. Cold gas is fed into the reactor and flows downward along the cold wall that is positioned opposite to the substrate. The gas moves upwards on the substrate side where it is heated, an effect which also drives the convection. Part of the gas leaves the reactor through the outlet while the portion far from the substrate stays in the convection roll for another turn. This corresponds to an internal 'recirculation' mechanism which reduces the amount of TCS that is required to grow a given layer thickness. It is easily understood that the inclination of the substrate and the bottom wall is crucial to the convection.

1.5.1.3 Batch type epitaxial reactors

Despite the tremendous progress achieved with the ConCVD and COCVD reactors there is still a long way to go before the reliability and safety of both concepts will be fully proven. In the microelectronics sector large vertical batch type furnaces, based on SiH_4 as Si-precursor, have been developed for 200 and 300 mm wafers with throughputs in the order of 100 wafers/h, which corresponds to 5 m^2/h. Adapting the poly-Si deposition processes for thicker poly-Si layers (like for power electronics applications) by using slightly higher temperatures (100–200 °C higher) and reducing the uniformity specs to 10 %, the required cost goals might also be attainable with such deposition systems.

The first indications that suitable epitaxial quality is reachable in such systems have been obtained in a batch type LPCVD system [92]. The system consists of a resistively heated quartz tube connected to a pump system at one end and closed with a quartz door at the other (the thermal insulation between door and reaction volume is realized by a vacuum-pumped quartz belljar). Si layers can be grown on 20 wafers simultaneously, using a system which allows removal of the unwanted Si deposition on the reactor walls by using a quartz insert which can be easily removed from the system. The wafers can be arranged in several configurations as shown in Figure 1.24a and b. The horizontal set-up results in a thickness variation below 20 % for five $5 \times 5\,cm^2$ samples, which is acceptable for solar cell applications. High quality epitaxial layers have been obtained, a fact illustrated by solar cells produced in layers grown on p^+-monocrystalline Si substrates [93]. For a process with a low deposition rate (between 20 and 50 nm/min) a defect density of 10^4 defects/cm^2 can be obtained. This value is comparable with

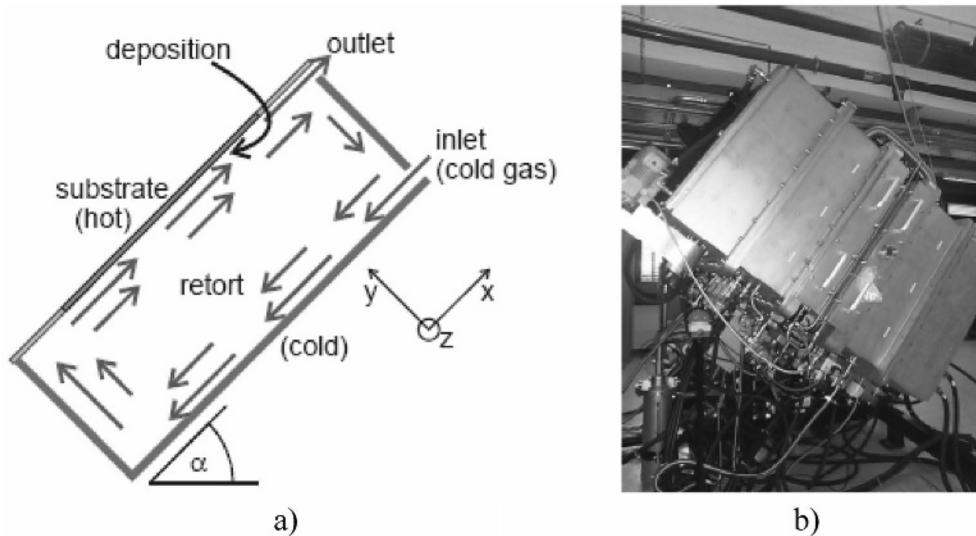

Figure 1.23 a) The concept of convection-assisted chemical vapor deposition. The flow of feed gas is enhanced and stabilized by thermal convection. The convection is governed by the reactor inclination angle α. Reproduced with the permission from Proc. 19th Europ. PVSEC, Paris, (2004), p. 1241. Copyright (2004) Thomas Kunz, ZAE Bayern e.V; b) Photograph of the new CVD system. Reproduced with the permission from Proc. PVSEC-15, Shanghai, (2005), p.190. Copyright (2005) Thomas Kunz, ZAE Bayern e.V.

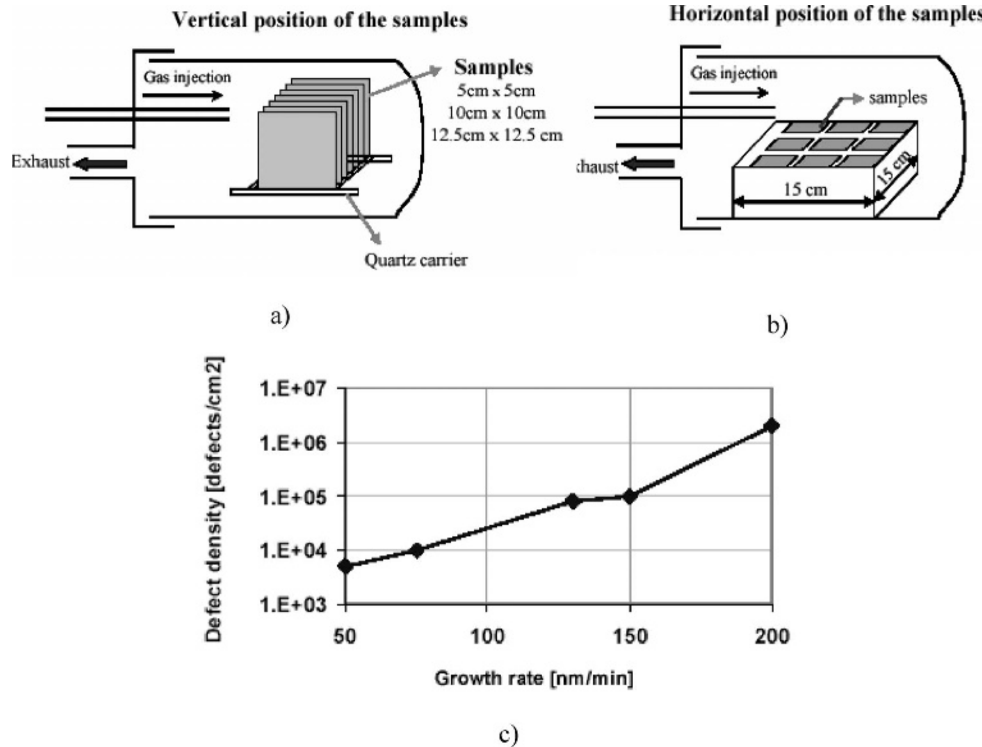

Figure 1.24 a) and b) Basic configuration of the LPCVD system and wafers stacking used in Reference [92] and [93] c) Dependence of the defect density on the deposition rate in the LPCVD-system.

the quality of the epitaxial layers on the same type of highly doped substrates grown in a commercial reactor. By increasing the partial pressure of the SiH_4 flow in the total gas flow, an increase in growth rate can be obtained. The defect density of the grown layers increase strongly as a function of the deposition rate as shown in Figure 1.24c.

An alternative batch type reactor concept is the so-called stacked epitaxial reactor [94] (SER) which is based on densely packed resistively heated graphite susceptors as shown in Figure 1.25a. The concept (shown in Figure 1.25b) is based on pioneering work in the eighties [95]. The shown configuration results in highly efficient and homogeneous heating. Presently, a prototype of this reactor is being built including a H_2 recirculation system. The required H_2 gas flow to the system is high to keep the temperature in the gas bulk sufficiently low as to avoid dust formation. Without H_2 recirculation, the economics of the approach would be endangered. The system is foreseen to operate at atmospheric pressure in a mass transport controlled regime, although in the prototype the possibility is foreseen to also operate at low pressure.

1.5.2 Liquid phase epitaxy reactor upscaling

For LPE reactor upscaling one can also make the same distinction between in-line concepts and batch type concepts. In general, the concepts have not yet reached the same maturity as the CVD concepts.

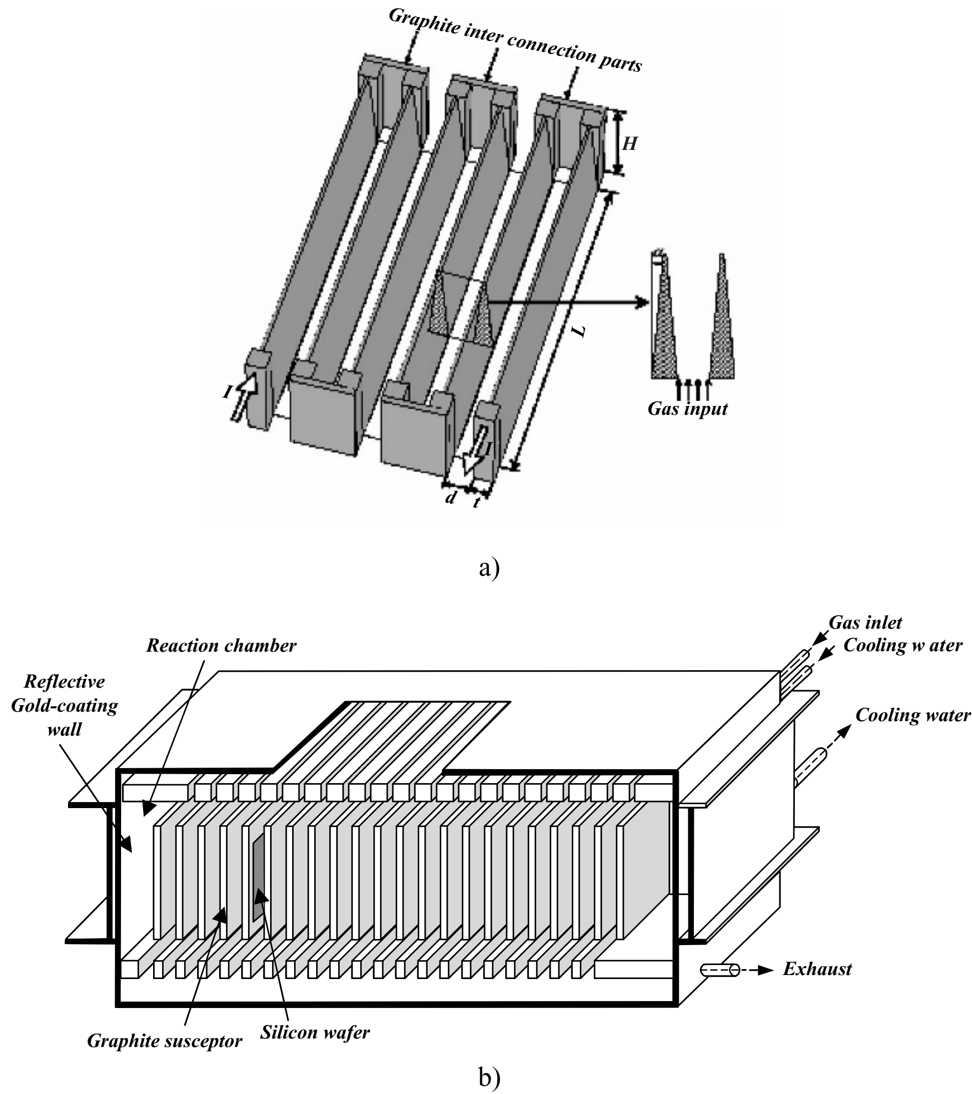

Figure 1.25 a) Graphite susceptor configuration in the SER reactor and detail of the cross-section of an interduct; b) Artists' view of the SER-concept.

1.5.2.1 Temperature difference method

The temperature difference method (TDM) is a promising quasicontinuous technology for the growth of thin film silicon from solution on large-area multicrystalline substrates ($10 \times 10\,\text{cm}^2$) [96, 97]. It was originally developed by Nishizawa [98] and has been used for the deposition of III-V semiconductor layers for luminescent devices. The thermodynamic driving

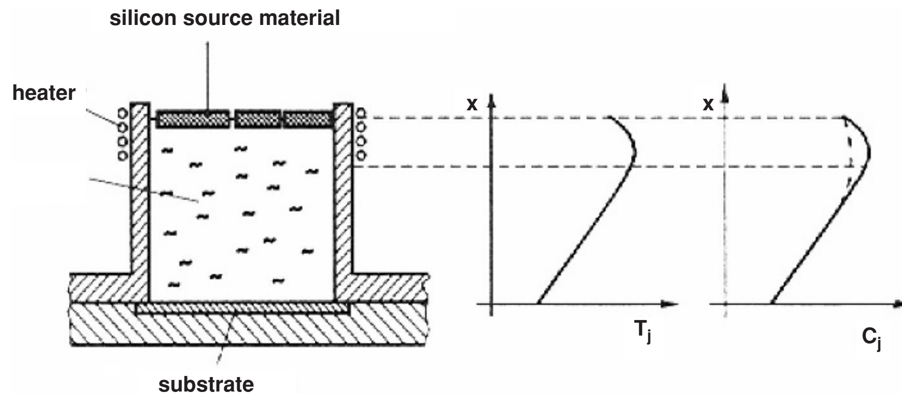

Figure 1.26 Principle of the temperature difference method (taken from reference [97]); the heater at the top ensures the temperature difference between source and substrate; Reproduced Figure 1 with permission from B. Thomas, G. Muller, P.-m. Wilde, and H. Wawra, Properties of silicon thin films grown by the temperature difference method (TDM), *Conference Record of the 26th IEEE Photovoltaic Specialists Energy Conference, Anaheim*, 771–774, 1997. Copyright (1997) IEEE.

force for layer growth by TDM is generated by a temperature gradient perpendicular to the substrate surface as shown in Figure 1.26. This temperature gradient results in a concentration gradient over the melt. This gradient is the driving force for layer growth on the substrate. Because the temperature remains constant during growth, the temperature dependence of the solubility does not influence the layer composition.

Silicon thin films have been grown from In/Ga solutions with growth rates up to 0.3 μm/min. Minority-carrier lifetimes of 5–10 μs were determined in 30 μm thick epitaxial layers both on mono- and multicrystalline Si substrates, which is remarkably high taking into account the absence of any H-passivation treatment

1.5.2.2 Batch type multiwafer liquid phase epitaxy system using melt-back

Standard LPE setups like the 'sliding boat approach' are not compatible with large batch type processes because of the necessity to change the solvent after each epitaxial growth as the amount of dissolved Si has diminished. The University of Konstanz is therefore developing a system, based on dipping the substrates into an 'infinite source' [99, 100], the principle of which is shown in Figure 1.27a. The present system (see Figure 1.27b) is capable of handling 16 substrates at a time, but there is no basic lemitation for further upscaling. An interesting asset of the proposed approach is the melt-back step, carried out before each growth process to supply silicon to the melt from the UMG-Si [100, 101] instead of adding electronic grade silicon to the solution. The upgrading of the Si material, done in this way, is probably more energy efficient than the purification of metallurgical grade Si. Small-area (3 cm^2) solar cells produced in these LPE layers by means of a solar cell process compatible with industrial practice showed efficiencies around 10 %.

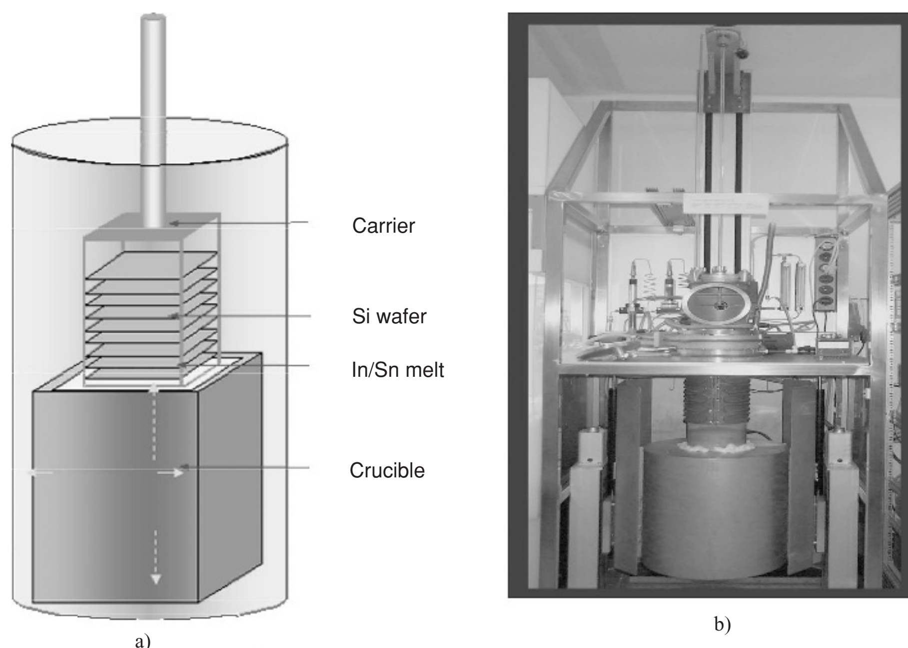

Figure 1.27 a) Schematic view on the batch-type LPE system based on dipping the substrates in an 'infinite source'. b) Present system. Courtesy of University of Konstonz.

1.6 CONCLUSIONS

Epitaxial thin film solar cells represent a technology that is very different from other thin film technologies but is rather close to the dominant bulk silicon solar cells. As such it is an appealing option in scenarios of gradual transition from wafer based solar cells to thin film monolithic modules. The potential cost reduction, while not as dramatic as for some other thin film technologies, is nevertheless substantial. Importantly, the technology would decrease the dependency of the PV industry on poly-Si feedstock. Thin film epitaxial cells show a high level of maturity, with industrial type solar cells reaching efficiencies of about 13 %. To further increase performance, optical confinement is necessary. Recent developments on buried porous silicon reflectors indicate that the path length enhancement necessary to reach efficiencies similar to those of bulk solar cells is achievable. Several deposition techniques have been investigated, but technologies based on thermal CVD are the most mature and give the best results. However, a prerequisite for future commercialization of the technology is the availability of a dedicated high throughput epitaxy system. This is therefore a very important topic in current epitaxial solar cell research and development.

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