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Introduction

1.1 IMPORTANCE OF TRADEOFFS AND OPTIMIZATION IN ANALOG CMOS DESIGN

Wireless, wire-line, and optical communications, along with entertainment, multimedia, biomedical, and many other applications, require analog circuits for interfacing with the physical world. The proliferation of these applications has resulted in a continual increase in the quantity and complexity of analog circuits fabricated in the prevalent, complementary metal–oxide semiconductor (CMOS), integrated circuit technology.

Analog CMOS design requires the design of system specifications and architectures, followed by the design of circuits containing various topologies of interconnected metal–oxide semiconductor, field-effect transistors (MOSFETs). Following this, the designer must select a drain current, channel width, and channel length for every MOSFET in a circuit. This book considers these MOSFET design selections.

In this book, the inversion coefficient[1] replaces channel width as a design choice because the inversion coefficient provides a numerical measure of metal–oxide semiconductor (MOS)[2] inversion where values below 0.1 correspond to weak inversion, values between 0.1 and 10 correspond to moderate inversion, and values above 10 correspond to strong inversion. Channel width, required for layout, is easily calculated from the selected drain current, inversion coefficient, and channel length and is implicitly considered in predictions of MOS performance.

The three independent degrees of MOS design freedom, whether drain current, inversion coefficient, and channel length used in this book, or the traditional choices of drain current, channel width, and channel length, influence all measures of MOS performance,[3] including physical size, gate–source bias and drain–source saturation voltages, small-signal parameters, signal distortion, intrinsic voltage gain, capacitances, intrinsic and extrinsic bandwidths, thermal noise, flicker noise, mismatch, and leakage. Performance such as capacitances, intrinsic voltage gain, and intrinsic bandwidth can vary over several

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[1] References for the inversion coefficient follow in Chapter 2, along with discussions of weak, moderate, and strong inversion.

[2] The abbreviations MOSFET and MOS are often used interchangeably, although MOS can include a broader definition beyond MOSFET devices alone.

[3] Chapter 3 describes measures of MOS performance in detail.

Tradeoffs and Optimization in Analog CMOS Design David M. Binkley

decades, resulting in a wide range of available circuit performance for a given circuit topology. Although three degrees of design freedom for each MOSFET in a circuit greatly complicate analog CMOS design, this affords significant opportunities to manage performance tradeoffs and optimize designs.

The subject of this book is guiding the designer in the selection of MOS drain current, inversion coefficient, and channel length for desired tradeoffs in performance leading towards optimum design. This is done through hand and spreadsheet expressions and graphical presentations of MOS performance that are valid in all regions of operation. A key aspect of this book is the detailed treatment of moderate inversion, which is increasingly important in low-voltage, low-power design. Operation in moderate inversion offers the advantages of low MOS drain–source saturation voltage, high transconductance efficiency (the ratio of transconductance to the drain bias current), moderate intrinsic bandwidth, and good immunity to velocity saturation effects that otherwise could deteriorate performance. Design in moderate inversion, with hand expressions recently facilitated by developments like the EKV MOS model,[4] is rarely covered in existing books and has traditionally required iterative computer simulations. This book complements existing books by specifically addressing tradeoffs and optimization of analog CMOS circuits in weak, moderate, and strong inversion, over the full range of process channel length. In addition to addressing common measures of performance like intrinsic voltage gain and bandwidth, this book contains considerable material addressing the tradeoffs and optimization of thermal noise, flicker noise, and mismatch.

The methods and design examples presented in this book are intended to help the designer manage performance tradeoffs and rapidly create optimum or near-optimum designs before launching the computer simulations required to verify a design for production. In the author's experience, this minimizes trial-and-error simulations, saves design time, provides a cross-check with production MOS models, builds design intuition, and enhances the enjoyment of design.

1.2 INDUSTRY DESIGNERS AND UNIVERSITY STUDENTS AS READERS

This book is written for the industry designer or university student familiar with the analysis and design of analog CMOS circuits using traditional, strong-inversion, square-law MOS modeling. The book hopes to extend this knowledge and enable design and design optimization freely in weak, moderate, and strong inversion, inclusive of small-geometry effects and other advanced effects like thermal noise, flicker noise, and mismatch. It is assumed that the reader is familiar with operational transconductance amplifiers, operational amplifiers, and other analog CMOS circuits along with their DC bias and small-signal analysis. While full details are provided for thermal- and flicker-noise analysis, it is also assumed that the reader is familiar with the basic concepts of noise analysis. These core analog CMOS design topics are covered in detail in a number of excellent books.

Most of the material contained in this book was used by the author at Concorde Microsystems[5] in the late 1990s for the design of front-end, CMOS integrated circuits for positron emission tomography (PET) medical imaging systems manufactured by Siemens. Some of the material has also been successfully taught several times in a course, *Advanced Analog CMOS Design*, at the University of North Carolina at Charlotte. Both in industry and at the university, the material was successful in minimizing time-consuming, trial-and-error circuit simulations by building design intuition and guiding the designer towards optimum design.

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[4] References for the EKV MOS model follow in Chapter 2.

[5] In 2005, Concorde Microsystems, Inc., became part of Siemens Medical Solutions.

1.3 ORGANIZATION AND OVERVIEW OF BOOK

This book begins by introducing the complexity of analog CMOS design resulting from the MOS design choices of drain current, inversion coefficient, and channel length. This is followed by an in-depth study of MOS performance and tradeoffs resulting from these design choices. The book then presents design examples of CMOS operational transconductance amplifiers optimized for DC, balanced, and AC performance, and micropower, low-noise, CMOS preamplifiers optimized for low thermal and flicker noise. Finally, the book concludes with a discussion on how the design methods can be extended to smaller-geometry CMOS processes as well as emerging non-CMOS processes.

The book is organized into two parts having emphasis on devices and circuits, respectively.

Part I, MOS Device Performance, Tradeoffs and Optimization for Analog CMOS Design, contains Chapters 2, 3, and 4 and is overviewed below.

Chapter 2, MOS Design from Weak through Strong Inversion, briefly introduces MOS operation in all regions, emphasizing decreasing transconductance efficiency at increasing inversion levels, including the additional decrease associated with small-geometry effects like velocity saturation. This chapter also introduces normalized MOS drain–source resistance as an Early voltage, which has a strong dependence on the channel length. The complexities associated with selecting MOS drain current, inversion coefficient, and channel length are compared to design using bipolar transistors where generally only the collector current must be selected. This emphasizes the importance of optimization methods that permit design freely in all regions of MOS operation, over the full range of channel length. The chapter concludes by presenting previously reported optimization methods, including both electronic design automation (EDA) and hand methods.

Chapter 3, MOS Performance versus Drain Current, Inversion Coefficient, and Channel Length, is an extensive “book within a book” chapter that is the basis for understanding MOS performance tradeoffs that lead the designer towards optimum design. The chapter begins by introducing the inversion coefficient as a primary design choice governing the region and degree of MOS inversion. The chapter describes the advantages of selecting MOS drain current, inversion coefficient, and channel length for design optimization, with channel width found from these design selections. Additionally, the chapter introduces the *MOSFET Operating Plane*, which illustrates tradeoffs in performance. For example, operation at low inversion coefficients in weak or moderate inversion at long channel lengths optimally maximizes voltage gain and minimizes gate-referred thermal- and flicker-noise voltage, mismatch, and the drain–source saturation voltage. This is referred to as a DC or low-frequency optimization. Conversely, operation at high inversion coefficients in strong inversion at short channel lengths maximizes bandwidth and minimizes transconductance distortion. This is referred to as an AC optimization. Operation at intermediate inversion coefficients and channel lengths provides a balance of DC and AC performance.

The majority of Chapter 3 presents expressions and design graphs of MOS performance versus the design choices of drain current, inversion coefficient, and channel length. Performance includes channel width and gate area, effective gate–source voltage, drain–source saturation voltage, transconductance efficiency, transconductance distortion, body-effect transconductance ratio, normalized drain–source resistance or conductance, intrinsic voltage gain, intrinsic and extrinsic capacitances, intrinsic and extrinsic bandwidths, thermal noise, flicker noise, mismatch, and leakage. Much of this material is based on or extended from the EKV MOS model and includes hand expressions, often with experimental validations. Simple hand model extensions are included for small-geometry effects like velocity saturation, vertical field mobility reduction, drain-induced barrier lowering, and increases in gate-referred flicker noise voltage with the inversion level. Although performance can be predicted and measured for any process, most validating experimental measurements are for a typical $0.18\,\mu\text{m}$ CMOS processes. Finally, the chapter contains predictions of gate leakage current and describes its effect on circuit performance. This can be significant for gate-oxide thickness less than around 2 nm.

Chapter 4, Tradeoffs in MOS Performance, and Design of Differential Pairs and Current Mirrors, presents tradeoffs of MOS performance versus the design choices of drain current, inversion coefficient, and channel length. Expressions and design graphs show tradeoffs in device channel width and gate area, effective gate–source bias and drain–source saturation voltages, intrinsic voltage gain, intrinsic bandwidth, capacitances, gate-referred thermal- and flicker-noise voltage, drain-referred thermal- and flicker-noise current, and gate–source voltage and drain current mismatch. Predicted and measured tradeoffs are given for a typical 0.18 μm CMOS process. Tradeoffs, for example in MOS intrinsic voltage gain and bandwidth, show that gain decreases while bandwidth increases as the inversion coefficient increases in strong inversion. These tradeoffs, however, are even more significant as channel length increases where voltage gain increases, but bandwidth decreases more rapidly. The chapter also shows tradeoffs in thermal noise efficiency, bandwidth-power-accuracy, and other figures of merit that combine multiple aspects of performance.

Chapter 4 concludes by illustrating performance tradeoffs through the design of differential pairs and current mirrors. This includes designs for separate design choices of the inversion coefficient, channel length, and drain current, and designs optimized for various tradeoffs in DC and AC performance at both millipower (100 μA) and micropower (1 μA) levels of drain current. The designs use the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet to show MOS performance for the selected drain current, inversion coefficient, and channel length. This spreadsheet is available at the web site for this book and is described in the Appendix.

Part II, Circuit Design Examples Illustrating Optimization for Analog CMOS Design, contains Chapters 5 and 6 and is overviewed below.

Chapter 5, Design of CMOS Operational Transconductance Amplifiers Optimized for DC, Balanced, and AC Performance, illustrates design optimization using two different operational transconductance amplifier (OTA) topologies in two different CMOS processes. Simple, 0.5 μm CMOS OTAs are described first where devices in a given version operate at equal drain currents, inversion coefficients, and channel lengths. This is typical of general-purpose designs where input devices do not dominate noise or mismatch and provide a simple design example for introducing the design methods. The OTAs are optimized for DC, balanced, and AC performance by operating devices at low, moderate, and high inversion coefficients with long, moderate, and short channel lengths. The DC-optimized OTA has high transconductance, output resistance, voltage gain, and input and output voltage ranges, combined with small input-referred thermal-noise voltage, flicker-noise voltage, and offset voltage due to local-area mismatch and systematic offset. The AC-optimized OTA has high transconductance bandwidth, combined with small transconductance, transconductance distortion, input and output capacitances, and layout area. The balanced optimized OTA has a balance of DC and AC performance.

Detailed circuit analysis and performance trends are developed, and device performance resulting from drain current, inversion coefficient, and channel length selections is mapped into OTA circuit performance using the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet. Measured voltage gain is 326, 110, and 16.8 V/V, transconductance bandwidth is 5, 51, and 350 MHz, input-referred flicker-noise voltage density at 100 Hz is 80, 450, and 2000 $\mathrm{nV/Hz^{1/2}}$, and input-referred offset voltage due to mismatch is 1.1, 2.2, and 10.2 mV (1σ) for the DC-, balanced, and AC-optimized OTAs, respectively. Measured transconductance is 912, 647, and 383 μS, input-referred thermal-noise voltage density is 11.2, 14.4, and 19.4 $\mathrm{nV/Hz^{1/2}}$, and the input, 1 dB compression voltage is 78, 115, and 218 mV. This illustrates the wide range of available performance tradeoffs. The OTAs operate at equal core (excludes bias references) supply currents of 200 μA and supply voltages of ±1.25 V, illustrating performance comparisons at equal power consumptions of 500 μW.

Chapter 5 also illustrates design optimization through the design of three, cascoded, 0.18 μm CMOS OTAs where devices in a given version operate at different drain currents and inversion coefficients so input devices dominate the thermal noise. The OTAs are optimized for DC, balanced, and AC performance by operating devices at fixed inversion coefficients with long, moderate, and short channel lengths. Again, detailed circuit analysis and performance trends are developed, and device performance is mapped into OTA circuit performance using the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet. Measured voltage gain is 19 100, 4400, and 490 V/V, transconductance bandwidth is 75, 285, and 850 MHz, input-referred flicker-noise voltage density at 100 Hz is 96, 420, and 1700 $\mathrm{nV/Hz^{1/2}}$, and input-referred offset voltage due to mismatch is 0.24, 1.1, and 3.2 mV (1σ) for the DC-, balanced, and AC-optimized OTAs, respectively. Operating input devices near the center of moderate inversion results in a nearly constant transconductance of 1900 μS, input-referred thermal-noise voltage density of 5 $\mathrm{nV/Hz^{1/2}}$, and input, 1 dB compression voltage of 55 mV. Although non-input devices do not have sufficient device area to ensure negligible flicker-noise and mismatch contributions, the measured input-referred offset voltage for the DC-optimized OTA is very low at 0.72 mV (3σ) and is more typical of that found in bipolar transistor circuits. The OTAs operate at equal core (excludes bias references) supply currents of 300 μA and supply voltages of ±0.9 V, illustrating performance comparisons at equal power consumptions of 540 μW.

Chapter 6, Design of Micropower CMOS Preamplifiers Optimized for Low Thermal and Flicker Noise, illustrates design optimization through the design of 0.35 μm, silicon-on-insulator (SOI), CMOS micropower, low-noise preamplifiers having differential and single-ended inputs. This chapter begins by describing performance measures useful for minimizing input-referred thermal-noise voltage for a given level of power consumption, and the preamplifiers presented here are compared to others reported in the literature. The chapter then presents methods for minimizing input-referred thermal- and flicker-noise voltage, including operating input devices in weak or moderate inversion for high transconductance and low input-referred thermal-noise voltage at minimum current consumption. Operating non-input devices well into strong inversion for low transconductance and low drain-referred thermal- and flicker-noise current is described to minimize non-input device noise contributions. The advantage of resistive degeneration of non-input device flicker noise is also presented, and noise is optimized against the constraints of available bias compliance voltage. This shows that managing non-input device noise becomes increasingly difficult at low supply voltages where bias compliance voltage is reduced.

After detailed circuit analysis for the differential and single-ended input preamplifiers, device performance resulting from device drain current, inversion coefficient, and channel length selections is again mapped into overall circuit performance using the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet. The measured input-referred thermal-noise voltage density is 63.8 and 35.3 $\mathrm{nV/Hz^{1/2}}$ and flicker noise at 1 Hz is 240 and 160 $\mathrm{nV/Hz^{1/2}}$, giving flicker-noise corner frequencies of 12 and 19 Hz for the differential and single-ended input preamplifiers, respectively. The preamplifiers operate at equal core supply currents of 2 μA, supply voltages of 3.3 V, and power consumptions of 6.6 μW, excluding bias references and optional output buffers.

Chapter 7, Extending Optimization Methods to Smaller-Geometry Processes and Future Technologies, concludes this book by discussing the extension of optimization methods to smaller-geometry CMOS processes and even emerging non-CMOS technologies like organic, thin-film and carbon nanotube, field-effect transistor technologies. Evaluating measures of performance like transconductance efficiency, normalized drain–source resistance, intrinsic voltage gain, capacitances, intrinsic bandwidth, noise, mismatch, and leakage in terms of device bias current, inversion level, and channel length permits ready extension of the methods. The technology normalization inherent in the inversion coefficient facilitates this extension.

1.4 FULL OR SELECTIVE READING OF BOOK

Recognizing that few industry designers or university students will have the time to read this book fully, it was written to be read either fully or selectively. The extensive use of design tables facilitates selective reading by summarizing predictions of MOS device and circuit performance, often with trends listed for the design choices of device drain current, inversion coefficient, and channel length. Additionally, figures facilitate selective reading by showing predicted and measured performance where trends and tradeoffs are readily observed. The figures contain narrative captions that, in addition to titling the figures, summarize key information. The tables and figures, with their captions, are intended to rapidly "tell the story" with the book text providing detailed, supportive information.

In addition to material provided in tables and figures, the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet permits the reader to rapidly estimate the performance of individual MOS devices and complete circuits as design choices are explored. This spreadsheet is used in the design examples presented in this book and can be extended to other designs by the reader. The spreadsheet, available from the book's web site, listed on the cover, is summarized in the Appendix.

A brief reintroduction of topics, symbols, abbreviations, and meanings within separate chapters also permits selective reading where individual chapters can be read with basic comprehension without requiring frequent reference to material contained in other chapters. Reference is made to previous material where the reader can obtain detailed explanations, derivations, measured data, and literature citations.

Finally, the table of contents facilitates selective reading where topics can be identified rapidly, while hopefully avoiding less efficient page searches using the *Index*. While many symbols and abbreviations are redefined in new chapters, these can also be found in the *List of Symbols and Abbreviations*.

1.5 EXAMPLE TECHNOLOGIES AND TECHNOLOGY EXTENSIONS

Design examples presented in this book are in 0.5, 0.35, and 0.18 μm CMOS processes, with most experimental measurements provided for a typical 0.18 μm CMOS process. At publication time, some designers in large companies are working in 0.09 and 0.065 μm processes, but many designers in smaller companies or those designing dedicated analog or mixed-signal integrated circuits are working in 0.18 μm or even larger feature size processes. Although not available for system-on-chips fabricated in the highest-density digital CMOS processes, except through thick gate-oxide options, many analog designers have a preference for the thicker gate oxide and higher supply voltages of 0.18 μm and larger processes.

Regardless of the CMOS process used, the performance trends and tradeoffs presented here guide the designer towards optimum design. For example, as described in Chapter 3, transconductance efficiency versus the inversion coefficient follows the universal behavior of being maximum in weak inversion, beginning to decrease in moderate inversion, and decreasing continually in strong inversion, decreasing faster for short channel lengths due primarily to velocity saturation. While this is illustrated in 0.5 and 0.18 μm processes here, the behavior is similar for smaller-geometry processes with transconductance efficiency decreasing faster for channel lengths below 0.18 μm. As discussed in Chapter 7, the inversion coefficient with its inherent technology normalization facilitates extending the methods presented here to smaller-geometry processes.

The hand expressions of MOS performance presented here can be extended for improved accuracy in smaller-geometry processes as long as these expressions are still simple enough to permit design guidance and intuition. Additionally, the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet is a "work in progress" that in the future could be coupled to the EKV MOS model or other simulation MOS models. This would permit MOS device and circuit performance prediction with improved accuracy in smaller-geometry processes. The reader is invited to check the book's web site for updates to the spreadsheet.

1.6 LIMITATIONS OF THE METHODS

This book presents approximate hand or spreadsheet expressions of MOS performance and resulting circuit performance as the designer explores device drain current, inversion coefficient, and channel length selections and makes initial, informed design choices. The expressions are necessarily simplified to show performance trends and tradeoffs useful to guide the designer towards an optimum or near-optimum design before launching computer circuit simulations. Although predictions of MOS transconductance, thermal noise, flicker noise, and mismatch are often within measured values by 10 %, errors in the prediction of drain–source resistance and resulting open-loop, circuit voltage gain can be greater. This is because of complex dependencies of drain–source resistance on the inversion level, channel length, and drain–source voltage. Fortunately, closed-loop circuit configurations are commonly used to desensitize circuit performance to variations in open-loop gain. The methods and expressions presented provide useful design guidance, especially since performance measures, like voltage gain and bandwidth, often vary over several decades with inversion coefficient and channel length selections.

The methods and expressions presented here involve quasi-static MOS modeling where the frequency of operation is sufficiently low such that device charges immediately track terminal voltages. The methods provide guidance up to frequencies of approximately 25 % of the intrinsic MOS bandwidth, which is developed in Chapter 3. Non-quasi-static extensions, for example where resistances are placed in series with intrinsic capacitances, can be envisioned, but are not developed here. Although the methods and expressions presented here are quasi-static and approximate, they do consider important small-geometry effects such as velocity saturation, vertical field mobility reduction, drain-induced barrier lowering, and increases in gate-referred flicker noise voltage with increasing inversion level. Additionally, the methods permit the inclusion of excess thermal noise through the use of modeling parameters.

For gate-oxide thickness around 2 nm and below, gate leakage current and the resulting gate–source conductance, gate shot- and flicker noise current, and increase in mismatch can become significant. As described in Chapter 3, smaller channel length and gate area may be required to balance the traditional improvements in gain, flicker noise, and local-area mismatch at increasing channel length and gate area with the deterioration of these associated with increasing gate leakage current caused by increasing gate area. The *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet does not include gate leakage effects, which are negligible for the device and design examples contained in this book. These effects, however, could be included in later versions of the spreadsheet.

The methods and expressions presented in this book do not replace production MOS models used in computer simulations that are critical to verify the performance of candidate designs. Such simulation models can include non-quasi-static effects, especially for radio frequency (RF) applications, and gate leakage current effects. As mentioned, the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet might later be linked to the EKV MOS model or other simulation MOS models. This could then provide prediction accuracies approaching that of computer simulations.

As mentioned at various places in this book and well known to experienced designers, all candidate designs must be thoroughly verified by computer simulations using MOS models with parameters appropriate for the production process. This normally involves extensive simulations, inclusive of layout parasitics, over nominal and corner process conditions, temperature, and supply voltage. Portions of the disclaimer below appear at various places in this book and in the *Analog CMOS Design, Tradeoffs and Optimization* spreadsheet as a reminder.

1.7 DISCLAIMER

The design tradeoff and optimization methods, predictions, examples, and measurements given in this book or its associated spreadsheet software are intended for design guidance only, not for actual design, and do not correspond to any particular CMOS fabrication process. The designer must independently validate designs using MOS models and parameters appropriate for the actual fabrication process used.

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