
Preface

Electrostatic discharge (ESD) phenomena have been known to mankind since the Greek Empire when Thales of Miletus, one of the Seven Sages of Greece, noticed the attraction of strands of hay to amber, leading to the coining of the word “electron.” In the 17th century, Gilbert and Cabeo addressed the attractive and repulsive nature of electricity. In the 18th century, a rapid increase of interest occurred for scientists in the understanding of electrical physics—Gray, du Fay, Nollet, Musschenbroeck, Franklin, Watson, Aepinus, Canton, Priestley, Cavendish, Galvani, Coulomb, Volta, Poisson, Faraday—and continued into the 19th century—Laplace, Gauss, Oersted, Ampere, Davy, Ohm, Green, Ostrogradsky, Henry, Lord Kelvin, Joule, Neumann, Weber, Thomson, Kirchoff, Stokes, Helmholtz, and Maxwell. It was the discoveries made in the 1820s by Oersted, Ampere, Davy, and Ohm that began the basic understanding of electrical circuits.

Electrical discharge and the guiding of electrical discharge (e.g., lightning) was of interest to Benjamin Franklin in the 1700s, with the invention of the lightning rod. The lightning rod was mankind’s first effort to guide the electrical discharge current of a lightning strike in a direction that would not harm structures. Today, in semiconductor chips, it is the role of the ESD protection networks to guide the current through a semiconductor chip to prevent the failure of circuits and the semiconductor chip. In that sense, ESD protection serves the role of lightning rods for nano-structures; the October 2002 Scientific American article on ESD protection entitled “*Lightning Rods for Nano-electronics*” was truly an appropriate analogy. The role of the semiconductor engineer and ESD design engineer is to fulfill this same objective of guiding the current in a place that does not harm the circuitry—but on a much more smaller scale and in a significantly more complex environment than a lightning bolt and a church steeple.

But today, the focus is on ESD protection in semiconductor chips and electronic chip design.

This is the second book in the ESD Series. The first book in the John Wiley and Sons, Ltd series on ESD protection, entitled *ESD: Physics and Devices*, will serve as a companion book to this text. As stated in the Foreword of *ESD: Physics and Devices*, not only there is a quest for the scientific understanding of ESD, but also there is a struggle in the way that the subject is taught and presented. At this time, there is only one university course in the world that teaches a semester course of this fast rising discipline of ESD phenomenon in semiconductor components – in National Chiao-Tung University in Hsin-chu City, Taiwan. Educational texts worthy of teaching at a university level are needed to teach and educate

engineers for ESD protection of components as well as professionals that are developing ESD devices, circuits, and implementation strategies. To date, ESD is taught in individual lectures, short courses, and tutorials. The teaching of a single lecture on ESD is inadequate to provide educational learning on ESD and ESD engineering; the teaching of a single lecture only trivializes the magnitude of the ESD discipline. Today, there are ESD books, but they are not structured for formal undergraduate or graduate courses suited for physicists, mathematicians, material science majors, or electrical engineering from a generalist perspective which would draw a wide interest across the materials and semiconductor community; the goal of the book *ESD: Physics and Devices* was an attempt to address this.

While the first book *ESD: Physics and Devices* was targeted for the semiconductor device physicist, the circuit designer, the semiconductor process engineer, the material scientist, the chemist, the physicist, the mathematician, the semiconductor manager, and the ESD engineer, a second book is needed to address the details of the ESD job ahead for the professional ESD engineer and the circuit design teams: the design team head designer, the semiconductor chip floor-plan engineer, the power bus design engineer, the I/O design team, the receiver circuit engineer, the off-chip (OCD) driver engineer, the phase lock loop (PLL) engineer, the packaging engineer, the analog team, the radio frequency (RF) design team, the modeling team, the device extraction team, the design rule checking team, the verification team, the kit release team, the ESD kit release team, the graphic technician, the ESD test engineer, quality, reliability, field application engineering, and foundry customers. For the circuit designer and the circuit design team, a text is needed to arm the circuit designer to achieve his objectives effectively. Today, there is only one book *Basic ESD and I/O Design* by S. Dabral and T. Maloney which is an excellent text for the I/O designer. But, to train an ESD engineer, a book is needed which goes much deeper into the ESD circuits and ESD response of I/O circuits.

The cross-discipline nature of the ESD phenomena makes it a difficult subject to teach unless it is taught from a cross-discipline perspective or as a series of disciplines which are woven together carefully to build the understanding from first principles. This same dilemma occurred in the early 1960s in the teaching of integrated semiconductor electronics. The Semiconductor Electronic Education Committee (SEEC) was formed to address how to teach an engineer integrated electronics in a world that separated the teaching of solid state physics, devices, and circuits. It was stated in the Foreword of the SEEC series: “the development of micro-miniaturization of electronic circuits has blurred the dividing line between the ‘device’ and the ‘circuit’ and thus has made it increasingly important for us to understand deeply the relationship between internal physics and structure of a device, and its potentialities for circuit performance.” It was at this junction that the initiative to establish a series of semiconductor books was taken, which integrated the understanding from the fundamentals of semiconductor physics to circuits in a coherent fashion where each book built on the prior book with a bottom-up approach. In the ESD discipline, this same dilemma holds true.

This motivated me to move forward on the concept of not a single book, but a book series on electrostatic discharge phenomena. The objective of the book series is to establish an educational framework to establish an ESD discipline based on integration of physics, devices and circuits—from the bottom upward—for a wide audience, not just ESD engineers and ESD designers.

From this motivation, the first book *ESD: Physics and Devices* addressed the solid state physics, electro-thermal physics, discharge phenomena, stability theory, ESD electro-thermal

models, and semiconductor device equations. Concepts, such as current constriction, ballasting, and the language of ESD, were introduced. The book segmented the semiconductor devices into the specific regions so as to provide a generalist approach. The book continued with specifics in the area of CMOS, silicon on insulator (SOI), silicon germanium (SiGe), silicon germanium carbon (SiGeC), and future devices such as strained silicon, FINFETs, and carbon nano-tubes.

In this book, *ESD: Devices and Circuits*, a balance is established between a generalist approach and practical implementation to make it applicable to semiconductor chip design. As in the first text, an understanding of the bridge between the microscopic and the macroscopic phenomena is important; one must bridge from the single contact hole to the package; the scale ranges from the device, the circuit, the package, to the system. This traverses both spatial and temporal processes. In the understanding of the time response and the ESD phenomena, the device response, the circuit response, and the semiconductor chip response are important. In the understanding of the spatial response, the distribution effects of the current and voltage are also critical to the understanding of ESD phenomena.

In the semiconductor industry, it is important for circuit designers also to understand the “ESD problem.” The days of the ESD engineer as “semiconductor alchemist” are quickly disappearing; brute force methods are too much risk, and for “on-the-job ESD training” there is no time left. In the semiconductor industry, it is still the objective to run the business, get out the designs, and ship products; in this process, there is no time for ESD mistakes or ESD-induced schedule delays or ESD-induced yield loss. Today, there is a higher necessity to educate the circuit design teams in ESD design, since failure is not an option.

In this textbook, *ESD: Devices and Circuits*, a first goal is to teach what is the essential objectives of ESD design. It is common misunderstanding what the goal of the ESD protection network is.

A second goal is to teach how ESD design practices are different from standard circuit design. In other words, how is this design practice different from all other design practices? ESD design practices involve coupling, decoupling, buffering, ballasting, triggering, shunting, and distributing; a goal of this book is to demystify the magic and show the bag of tricks in the tool box that are commonly used. So, a goal is to teach a new method of design—ESD design—which consists of coupling solutions, decoupling solutions, buffering, ballasting, and a large collection of creative techniques.

A third goal is to show that there are many ways to achieve good ESD protection through circuit design practices. A famous Chinese expression is “It does not matter if it is a white cat, or a black cat, as long as it catches mice.” With ESD design, there are many ways to achieve the goals, which make the profession full-of-room for creative solutions. A goal of this book is to educate the reader to a point that they can evaluate the pros and cons depending on what his objective is.

A fourth goal is to show that there is not one method but many methods to achieve good ESD results. Good ESD results can be achieved through semiconductor process choices, through the circuit topology choice, or both. It is a common misunderstanding that ESD results are a function of only the semiconductor process. It is also common that the ESD engineer only addresses the ESD networks, and does not look at the circuits. This is a common problem today in the way that the semiconductor foundry–customer relationship is being addressed; the circuit designers are not showing the foundry the circuits, but expect it to solve or assure good ESD protection.

A fifth goal is to show how to design ESD networks. Some of the early chapters focus on design aspects down to the contact, and work up to the full-scale structure. One of the objectives is to focus on the design aspects and how they are different from standard design and design layout. These sections are relevant to both the ESD circuit and the I/O circuit.

A sixth goal is to show how to design better I/O circuits (e.g., not the ESD networks) and expose circuit designers to new circuits that can have ESD concerns. In this book, we are going to focus on how to improve the OCD circuit, receivers, differential receivers, and other circuits. One of the objectives is to teach how to provide more robust ESD networks *without* performance impacts. My first lesson in circuit design showed that to achieve an objective for reliability does not always mean a performance degradation; if you are creative, you can improve the performance or find a way not to impact the performance. My personal goal as an ESD engineer was to find circuit solutions that did not impact the performance, but improved the ESD protection. In this goal, some circuit inventions will be shown to demonstrate this concept.

A seventh goal is to show examples from bulk CMOS technology, silicon on insulator (SOI) technology, silicon germanium (SiGe) technology, silicon germanium carbon (SiGeC) technology, and gallium arsenide (GaAs) technology. Although a CMOS engineer may never work in the other technologies such as SOI, it is valuable to see how the technologies influence the ESD results, circuit designs, and solutions. Hence, it was a goal and objective to include circuit chapters in the other technologies to reinforce the ESD design practices and principles.

An eighth goal is to expose the reader to the patent art in the ESD field. A significant amount of activity in the ESD field can be found by reading the patent art. As a result, a number of patents are referenced which are either first in the field, relevant in the discussions of interest, or teach methods and methodologies.

The second book in this series, *ESD: Circuits and Devices*, will contain the following:

Chapter 1 introduces the reader to think about the role of resistance, capacitance, and inductance in the ESD design of semiconductor chips. Given resistance, capacitance, and inductance, which is the most important? Under what circumstances? Under what time constants? Device, circuit, and chip-level effects exist during ESD events. What are the ESD metrics on a device level? How would they differ on a circuit level? . . . and, what is the important ESD metrics on the ESD chip level? The question of how the voltage and current distribute within the device, the circuit, and the semiconductor chip or system is addressed. What are the current loops? What is the path of current flow in an ESD event, and what are the most important parameters? How does one analyze the current flow through the current loop? . . . and how does the current flow through the system? An “ESD Ohm’s Law” will be highlighted as a quick simple solution for quick circuit design “sizings” for evaluation of success or failure. The spatial distribution within the device, circuit, or chip is discussed. Lumped versus distributed circuits will be reviewed. Additionally, ESD metrics and ESD business strategy will be discussed.

Chapter 2 will be an elementary high-level perspective of how to “floor plan” a semiconductor chip, taking into regard the essential elements to achieve good ESD protection. Additionally, the chapter will discuss electrical and spatial connectivity. It is common working with ESD engineers and circuit designers that they are not thinking about whether the issue is a spatial issue or an electrical issue. From a top-down perspective, good ESD protection begins with a design team when it is built-in to the high-level floor plan prior to the semiconductor chip definition. This will serve as a brief introduction to ESD devices,

guard rings, pads, ESD input circuits, ESD power clamps, peripheral I/O versus array I/O footprint issues, and all the items to construct a good ESD strategy for ESD protection. Hence, there is a relationship between the electrical connectivity, the spatial connectivity, and the floor planning and integration of a single chip or system-on-chip (SOC) integration.

Chapter 3 begins the discussion of the design and layout of semiconductor devices. The chapter will focus on the ESD design of metal oxide semiconductor field effect transistors (MOSFET). In ESD design of MOSFET structures, all the physical dimensions and spacings have a role in the ESD operation; channel length, channel width, and contact spacing (contact-to-contact, contact-to-gate, contact to diffusion edge, and the “last” edge contact). Wiring a MOSFET for the optimum ESD protection is an art form in itself. The effect of broadside wiring, “parallel,” and “anti-parallel” wiring design addresses MOSFET wiring optimization as well as reinforcing the issue of the current and voltage distribution within a semiconductor device, as discussed in Chapter 1. The discussion continues to address the design layout and ESD issues for the “multi-finger MOSFET.” The multi-finger MOSFET issue addresses how the current and voltage distributes within a given MOSFET layout between a plurality of MOSFET fingers. Additionally, the chapter will address the issue of a plurality of MOSFETs in series or the series “cascode” MOSFET. The chapter will close on the issue of the ESD scaling issues of MOSFETs.

Chapter 4 focuses on the ESD design and layout of diode elements. The chapter will address diode elements typically found in CMOS and BiCMOS technology. These consist of LOCOS and STI-defined elements, as discussed in the first textbook *ESD: Physics and Devices*: p^+/n -well diodes, n^+/p^- substrate diodes, n -well/ p^- substrate diodes, polysilicon-bound diodes, and trench-bound diode elements. The physical dimensions and spacings of the diode elements and how they influence ESD operation will be the key focus of the chapter. In the p^+/n -well diode element, the issues of width effect, perimeter-to-area ratio, diode end effects, lateral ballasting, contacts, and wiring configurations are addressed. As in the MOSFET, the voltage and current distribution within the physical structure influences the ESD efficiency and how much area is utilized for ESD protection; this influences the ESD metric for the device. As in Chapter 3, the multi-finger p^+/n -well diode issue is addressed. Likewise, the physics, layout, and design of a plurality of p^+/n -well diodes in series are discussed. These will be referred to as “diode strings.” In this discussion, the issues of area ratio of successive stages, diode sharing, and different design architectures will be discussed. Triple-well “diode string” implementations will also be discussed.

Chapter 5 will discuss the ESD design and layout of SOI ESD elements. First, we will discuss the SOI polysilicon-bound gated-diode structure, also known as the lateral unipolar bipolar transistor (Lubistor). Second, we will discuss the dynamic threshold MOS (DTMOS) body- and gate-coupled diode ESD element. The SOI buried resistor (BR) element will also be discussed, as well as the unique issues associated with these elements for SOI technology.

In Chapter 6, the focus switches to semiconductor OCD circuit design and ESD issues. Various types of CMOS OCD circuit types will be discussed from asymmetric and symmetric CMOS, TTL, Gunning transceiver logic (GTL), open-drain, HSTL, and SSTL OCDs. Additionally, MVI drivers will be discussed. These include series stacked MOSFET pull-ups and pull-down CMOS OCDs, as well as self-biased n -well OCDs. Universal OCD circuits and the ESD implications will also be discussed. Additionally, programmable impedance OCDs networks will be discussed, as well as the ESD implications that they establish.

Chapter 7 will discuss semiconductor receiver circuits and ESD issues, Starting with a receiver and a single inverter followed by successively more complicated networks. ESD issues with full-pass transmission gates (TG), half-pass TG, and finally TG and feedback “keeper” networks. Solutions to address the receiver issues, with the introduction of the CMOS receiver with modified keeper networks, will also be introduced. Zero-threshold voltage half-pass TG receivers, pseudo-zero threshold voltage receivers, and the unique ESD issues will also be highlighted. CMOS receiver networks with feedback elements, such as Schmitt trigger networks and ESD issues, will be discussed. The issue of HBM and CDM solutions and integration with the receiver network will be also discussed. For effective receiver design, one must integrate the HBM and CDM solutions that are naturally integrated as not to impact receiver performance.

Chapter 8 focuses on SOI circuits. In this chapter, SOI ESD devices for receiver and OCD networks are discussed. SOI ESD double-diode designs, SOI ESD diode-strings, and SOI ESD MOSFET design will be shown. SOI ESD failure mechanisms will be discussed, and solutions to alleviate SOI ESD design failures will be reviewed. A new SOI double-diode gate-isolated ESD network design and method will be discussed. Additionally, SOI failure mechanisms in receiver network in half-pass TG, SOI BR resistors, and other elements will be discussed. Additionally, special networks, such as fuse circuitry and other issues, will be highlighted.

Chapter 9 addresses ESD power clamp circuits. ESD power clamps are used between the power supply rails to lower the chip impedance during ESD events. This chapter addresses CMOS, bipolar, and BiCMOS ESD power clamps, which are triggered by voltage conditions or frequency discrimination. The chapter will first discuss CMOS ESD power clamps that are commonly used in the semiconductor industry; these include grounded-gate NMOS clamps, gate-coupled MOSFETs, RC-triggered MOSFETs, substrate-triggered MOSFET ESD power clamps, and gate- and substrate-coupled MOSFET power clamps. Additionally, RC-triggered MOSFETs for mixed-voltage applications will be discussed. ESD power clamps for bipolar technology, suitable for silicon, silicon germanium, silicon germanium carbon, gallium arsenide, and indium phosphide technologies, will be discussed. The bipolar classes of power clamps discussed include both forward-bias and reverse-bias breakdown trigger networks as well as capacitively triggered networks; these include diode string trigger networks, Zener-breakdown triggered power clamps, and BV_{CEO} -breakdown-triggered power clamps. Triple-well ESD power clamps will also be discussed.

In this text book, I weave between theoretical, analytical, experimental, and practical considerations. The topics change from ESD layout, to circuit theory, to ESD phenomena, to floor plans, to space, and to time, changing scope, and scale. At times, I provide great analytical details, and then in some sections, teach by example of practical implementations. This is done intentionally. One must realize this is the nature of the ESD engineer, and the nature of the semiconductor industry.

Enjoy the text, and enjoy the subject matter of ESD. There is still so much more to learn.

B”H
Steven H. Voldman
IEEE Fellow