

Index

- Abstraction level, 43, 68, 77, 87, 94, 97
Analog, 1, 12, 14, 20, 41, 49, 50, 56, 65, 66, 67, 68, 73, 92, 102, 107, 108, 128, 129, 131, 138, 165, 171, 173
Antenna, 68, 76, 80, 104, 124, 125, 126, 127, 128, 157, 179
ASIC, 9, 10, 11, 12, 60, 73, 74, 75, 77, 79, 81, 82, 83, 87, 91, 92, 94, 98, 103, 104, 106, 111, 143, 162, 172, 173, 187, 189
ATPG, 105, 113, 182, 183

Back annotation, 68, 156
Base layer, 9, 10, 20, 21, 100, 101, 126
biCMOS, 5, 7
Bipolar, 5, 7, 77
BIST, 112

CAD, 73, 76, 78, 104, 155, 156
Chip, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 19, 21, 24, 26, 27, 28, 29, 33, 34, 36, 37, 38, 41, 44, 45, 46, 47, 48, 49, 51, 52, 54, 55, 56, 57, 58, 59, 60, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 73, 74, 75, 77, 78, 79, 80, 81, 82, 83, 84, 86, 88, 91, 94, 97, 98, 99, 100, 101, 102, 103, 104, 106, 112, 113, 115, 116, 117, 118, 119, 120, 121, 123, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 136, 137, 138, 139, 140, 142, 143, 145, 146, 147, 149, 150, 151, 152, 154, 155, 156, 157, 159, 161, 163, 164, 165, 167, 169, 171, 172, 177, 178, 181, 184, 185, 186, 187, 188, 189

Clock, 3, 4, 5, 13, 14, 54, 55, 56, 67, 69, 76, 78, 80, 83, 85, 94, 106, 111, 112, 123, 124, 126, 128, 129, 130, 133, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 164, 165, 166, 167, 168, 169
Clock insertion delay, 145
Clock sink, 143, 145, 146, 147
Clock skew, 129, 143, 144
Clock tree, 80, 111, 129, 139, 140, 141, 142, 143, 145, 146, 147, 148, 149, 164, 165, 169
CMOS, 1, 2, 5, 6, 7, 8, 14, 17, 19, 21, 23, 30, 37, 57, 58, 66, 67, 77, 102, 121, 122, 124, 161, 174, 180
Code coverage, 87, 89
Codesign, 5, 49, 51, 52, 53, 54, 86
Constraint, 5, 11, 52, 53, 63, 68, 70, 91, 92, 128, 130, 132, 145, 165, 166, 169, 174, 175, 177, 179
Controllability, 114, 116, 117, 149
Cost, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 15, 16, 17, 24, 33, 36, 37, 49, 50, 52, 53, 66, 69, 81, 83, 90, 102, 105, 119, 120, 162, 163, 165, 175, 183, 186
Cross talk, 4, 23, 45, 76, 80, 124, 125, 126, 128, 157
CTS, 129

Delay, 4, 44, 55, 56, 67, 75, 93, 105, 125, 129, 130, 131, 143, 144, 145, 146, 147, 152, 153, 154, 155, 156, 157, 158, 165, 166, 167, 168, 169, 172, 173, 174, 175, 176, 177, 178
Delay calculation, 155, 156

- Design reuse, 5, 50, 51
- Detailed route, 135, 136, 137
- DFM, 61, 62, 78
- DFT, 46, 76, 78, 111, 112, 113, 117, 119, 120, 123, 149
- Die, 24, 26, 27, 34, 36, 47, 48, 49, 50, 76, 78, 81, 91, 102, 118, 124, 127, 128, 179, 184, 185, 186
- DPPM, 47, 117, 118, 119, 120
- DRC, 179, 181, 182
- DV, 179

- EDA, 16, 51, 56, 67, 68, 69, 80, 91, 97, 125, 162, 187
- Electrical effort, 174, 175
- Electromigration, 4, 21, 45, 62, 80, 104, 125, 126, 129
- Equivalence check, 81, 163, 164
- ESD, 3, 4, 45, 63, 68, 76, 80, 104, 124, 157
- ESL, 44, 85, 86
- Extraction, 68, 76, 124, 149, 152, 153, 154, 155, 181

- Fault, 90, 112, 113, 115, 116, 117, 118, 119, 182, 183, 186
- Fault coverage, 112, 115, 116, 117, 118, 119, 183
- Floorplan, 76, 78, 81, 91, 97, 124, 128, 130, 131
- Flow, 20, 33, 45, 52, 61, 73, 74, 75, 76, 77, 80, 81, 126, 136, 137, 159, 187
- Formal verification, 42, 55, 68, 87, 163
- FPGA, 9, 10, 11, 14, 87, 163
- Functional coverage, 89, 90, 164

- GaAs, 5, 8
- Gate count, 91, 111, 128
- GDSII, 60, 61, 76, 123, 126, 179, 184
- Global route, 134
- GOI, 4, 45, 62, 68, 104, 157
- GV, 179

- Hard macro, 92, 130, 131, 133
- HDL, 42, 43, 44, 51, 85, 86, 88, 89, 92, 93, 94, 97, 105, 106
- hierarchical, 78, 91, 107, 127, 128, 130, 133
- hold, 145, 168, 169

- I/O, 5, 11, 36, 49, 76, 78, 91, 111, 112, 124, 128, 129, 130, 132, 145, 157, 161

- Implementation, 4, 9, 10, 11, 12, 15, 16, 45, 52, 54, 59, 67, 73, 75, 77, 78, 79, 80, 81, 83, 85, 86, 91, 92, 93, 94, 97, 100, 102, 103, 104, 105, 106, 107, 112, 130, 131, 139, 163, 164, 165, 173, 175, 177, 178, 179, 187, 188
- Integrated circuit, 1, 6, 7, 10, 11, 12, 17, 26, 28, 29, 33, 45, 55, 92, 113
- Integration, 1, 4, 5, 9, 12, 15, 44, 50, 65, 67, 68, 70, 77, 79, 80, 82, 84, 85, 88, 107, 124, 138, 165, 174, 187, 188
- IP, 14, 44, 51, 70, 87, 91, 92
- IR drop, 4, 45, 49, 68, 76, 80, 124, 127, 129, 136, 137, 157, 159, 160, 161, 162

- Latch-up, 3, 4, 7, 46, 68, 76, 80, 104, 124, 157
- Layout, 7, 10, 12, 42, 45, 51, 60, 61, 67, 68, 75, 76, 78, 79, 92, 97, 98, 99, 100, 102, 103, 111, 112, 121, 123, 124, 127, 128, 131, 133, 134, 146, 147, 152, 157, 158, 163, 164, 171, 172, 178, 179, 180, 181, 182, 184, 187
- Leakage, 5, 7, 8, 48, 57, 58, 59, 60, 63, 70, 106, 121, 123
- Length skew, 145, 146, 147
- Library, 10, 11, 68, 75, 86, 91, 92, 94, 97, 98, 103, 104, 105, 106, 111, 140, 169, 173
- Life span, 46, 62, 129, 138
- Logic effort, 104, 125, 174, 175, 176, 177
- LVS, 76, 79, 124, 181, 182

- Manufacturing, 5, 8, 10, 12, 16, 24, 32, 33, 42, 46, 60, 62, 63, 64, 65, 66, 68, 74, 75, 76, 78, 79, 88, 100, 102, 118, 125, 126, 156, 157, 163, 165, 178, 179, 180, 182, 184, 185, 186
- Market, 4, 9, 11, 15, 16, 51, 52, 70, 71, 74, 75, 76, 81, 82, 83, 86, 165, 186, 189
- Mask, 10, 12, 16, 18, 21, 28, 29, 30, 31, 32, 60, 101, 102, 125, 126, 184
- Metal layer, 7, 9, 10, 20, 22, 50, 97, 100, 101, 126, 127, 134, 135, 180

- Netlist, 11, 43, 51, 75, 76, 78, 79, 80, 91, 92, 94, 105, 106, 107, 109, 110, 111, 112, 123, 124, 128, 131, 139, 152,

- 162, 163, 164, 172, 173, 178, 181, 182, 184, 187
- NMOS, 7, 17, 19, 20, 46, 100, 102, 103
- NRE cost, 10, 11
- Observability, 42, 114, 116, 117, 149
- OPC, 60, 61, 126
- Package, 3, 28, 33, 34, 35, 36, 37, 38, 39, 40, 49, 50, 64, 68, 83, 91, 103, 127, 128
- Parasitic, 46, 68, 76, 121, 124, 125, 127, 128, 152, 153, 154, 155, 156, 163, 165, 172
- Path, 36, 44, 45, 46, 125, 131, 149, 157, 165, 167, 168, 169, 172, 173, 175, 177, 183
- PG, 79, 184
- Physical design, 14, 51, 112, 123, 124, 125, 127, 128, 129, 131, 138, 145, 164, 173, 177, 184
- Physical synthesis, 123
- Physical verification, 68, 73, 74, 178, 179, 181
- Place and route, 10, 11, 12, 44, 61, 68, 73, 74, 75, 76, 77, 78, 81, 97, 100, 105, 112, 124, 127, 130, 131, 155, 156, 157, 158, 165, 166, 187
- Placement, 11, 76, 97, 124, 128, 129, 131, 132, 133, 134, 139, 143, 151, 156
- Platform ASIC, 10, 11
- PMOS, 7, 17, 19, 20, 46, 62, 100, 102, 103
- Power consumption, 5, 6, 7, 8, 48, 52, 56, 57, 58, 69, 70, 83, 106, 120, 121, 122, 123, 128
- Power network, 127, 129, 135, 136, 137, 138, 139, 140, 157, 159
- Process, 4, 5, 6, 7, 10, 11, 12, 17, 18, 19, 20, 23, 26, 28, 33, 41
- Processor, 4, 12, 14, 16, 49, 51, 52, 54, 65, 69, 70, 84, 130, 133
- PSM, 60, 126
- Reliability, 12, 23, 24, 45, 47, 62, 63, 64, 68, 83, 125, 179
- Route, 11, 14, 37, 133, 134, 135, 138
- RTL, 11, 12, 15, 16, 44, 68, 73, 74, 75, 76, 77, 78, 80, 85, 86, 87, 89, 92, 93, 94, 95, 105, 107, 109, 123, 163, 164, 171, 173, 187
- SAF, 112, 113, 114, 115, 116, 117, 118
- Scan chain, 80, 112, 116, 117, 149, 150, 151, 152, 164
- Scan chain reorder, 80, 151, 152, 164
- Schematic, 68, 79, 97, 105, 107, 108, 109, 110, 111, 112, 178, 179, 181, 182
- SDF, 76, 124, 156, 172
- Setup, 145, 169
- Signal integrity, 49, 156, 157
- Silicon, 1, 3, 5, 6, 8, 15, 17, 18, 19, 21, 24, 25, 26, 28, 29, 33, 45, 51, 52, 69, 73, 75, 82, 83, 84, 98, 100, 102, 104, 106, 107, 112, 123, 126, 158, 162, 163, 175, 176, 177
- Simulation, 42, 43, 61, 68, 74, 87, 88, 90, 94, 96, 97, 105, 113, 123, 127, 155, 156, 163, 164, 165, 166, 167, 169, 171, 172, 173, 178, 187
- SiP, 40, 49, 50
- SoC, 1, 4, 5, 10, 12, 13, 14, 15, 16, 41, 44, 49, 50, 51, 52, 54, 55, 56, 65, 66, 67, 68, 69, 70, 80, 81, 84, 85, 88, 90, 102, 107, 123, 125, 129, 131, 138, 162, 164, 165, 172, 173, 174, 177, 182, 189
- Soft macro, 92
- Software, 3, 5, 13, 14, 15, 16, 51, 52, 53, 54, 65, 69, 70, 73, 76, 84, 85, 86, 173, 179, 181
- SOI, 5, 7, 8, 64
- STA, 55, 80, 156, 165, 167, 168, 169, 170
- Standard cell, 9, 10, 11, 12, 75, 94, 97, 98, 99, 100, 102, 103, 104, 105, 111, 121, 128, 131, 132, 133, 136, 150, 171
- SV, 181, 182
- Synchronous, 13, 54, 55, 56, 167, 172, 183
- Synthesis, 10, 11, 44, 68, 73, 74, 75, 76, 77, 78, 86, 91, 93, 94, 97, 104, 105, 106, 109, 111, 112, 123, 125, 128, 129, 139, 145, 151, 155, 163, 164, 165, 166, 172, 173, 174, 187
- Tapeout, 12, 21, 73, 74, 79, 162, 184
- Test bench, 43, 74, 87, 88, 89, 90, 163, 164
- Test coverage, 151
- Testability, 5, 46, 47, 52, 68, 73, 78, 83, 111, 114, 118, 119, 149
- Time skew, 145, 146, 147

- Timing closure, 4, 55, 80, 125, 145, 169, 173, 174, 177, 178
- Verification, 4, 10, 15, 41, 42, 43, 44, 51, 52, 54, 55, 60, 68, 73, 74, 75, 86, 87, 88, 90, 91, 92, 97, 105, 162, 163, 164, 165, 169, 178, 179, 181
- Verilog, 74, 85, 86, 88, 92, 107, 162, 172
- VHDL, 74, 85, 86, 88, 92, 94, 162, 172
- VLSI, 1, 3, 9, 16, 17, 19, 41, 44, 46, 48, 54, 55, 56, 57, 58, 60, 62, 64, 112, 120, 123, 124, 128, 129, 133, 159, 162, 165, 187
- Wafer, 8, 17, 18, 19, 21, 24, 25, 26, 27, 28, 29, 30, 31, 32, 47, 48, 63, 64, 100, 118, 184, 185
- Yield, 30, 45, 50, 60, 61, 62, 78, 80, 104, 118, 152, 177, 179, 181, 184, 185, 186, 187