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# 1 Introduction

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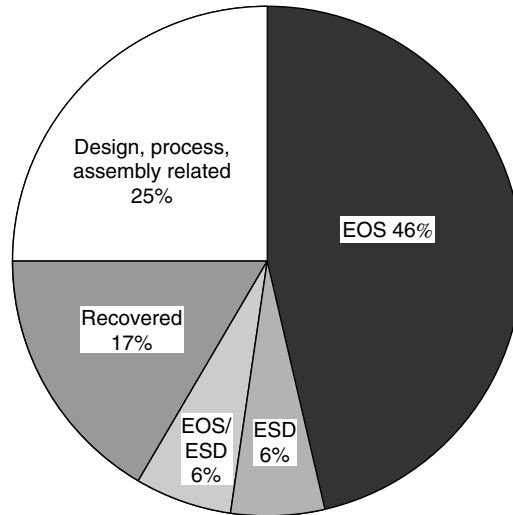
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## 1.1 BACKGROUND

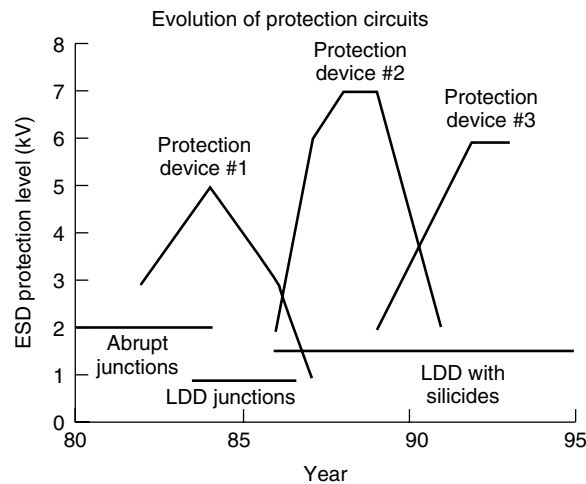
The phenomenon of electrostatic discharge (ESD) gives rise to images of lightning strikes or the sparks that leap from one's fingertips when touching a doorknob in dry winter. The sparks are the result of the ionization of the air gap between the charged human body and the zero-potential surface of the doorknob. Clearly a high voltage discharge takes place under these circumstances with highly visible (and sometimes tangible) effects. In the semiconductor industry, the potentially destructive nature of ESD in integrated circuits (IC) became more apparent as semiconductor devices became smaller and more complex. The high voltages result in large electric fields and high current densities in the small devices, which can lead to breakdown of insulators and thermal damage in the IC. The losses in the IC industry caused by ESD can be substantial if no efforts are made to understand and solve the problem [Wagner93]. Figure 1.1 shows that the distribution of failure modes observed in silicon ICs and ESD is observed to account for close to 10% of all failures [Green88]. The largest category is that of electrical overstress (EOS), of which ESD is a subset. In many cases, failures classified as EOS could actually be due to ESD, which would make this percentage even higher [Merrill93].

The significance of ESD as an IC failure mode has led to concerted efforts by IC manufacturers and university research workers in the US, Europe, and Japan to study the phenomena. Progress has been made in understanding the different types of ESD events affecting ICs, which has enabled test methods to be developed to characterize their ESD [Bhar83][Greason87]. ESD prevention programs have been put in place during IC manufacturing, testing, and handling, which have reduced the buildup of static and the exposure of ICs to ESD. Studies have been made of the nature of destruction in IC chips and, based on this work, techniques for designing protection circuits have been implemented, which has made it possible for the present generation of complex ICs to be robust for ESD.

The introduction of each new generation of silicon technology results in new challenges in terms of ESD capability and protection circuit design. Figure 1.2 shows how ESD performance for specific protection circuits has changed over time. Initially the ESD performance improves as the circuit designs mature and problems are solved or debugged. After a certain time the technology changes



**Figure 1.1** Distribution of failure models in silicon ICs. ESD accounts for approximately 10% with EOS responsible for close to 50% of the failures (After [Green88])



**Figure 1.2** ESD protection levels as a function of time. As technologies change, new protection devices are needed to reach the same ESD levels as before

(i.e., LDD, silicides) cause the circuit to no longer function to its original capability, and the introduction of new protection techniques are needed to restore good ESD performance. CMOS ICs in automotive environments require very high ESD protection levels, which places an even higher demand on the design of protection circuits. The speed with which new technologies are introduced have reduced the

available time for protection circuit development. In fact it is becoming more and more important to design circuits that can be transferred into the newer technologies with minimum changes. Hence, it is necessary to understand the main issues involved in ESD protection circuit design and the physical mechanisms taking place in order to ensure that the design can be scaled or transferred with minimum impact to the ESD performance. The purpose of this book is to provide an introduction to the basic mechanisms involved in ESD events, the physical processes taking place in the semiconductor, and the design and layout approaches to obtain good ESD performance.

The importance of building-in reliability demands design approaches that include ESD robustness as part of the technology roadmap.

The design and optimization of circuits with ultrasmall transistors (sub-0.25  $\mu\text{m}$ ) use a large number of simulation tools prior to committing the circuits to silicon. Thus, modeling and simulation of ESD effects in the protection circuit is important; we discuss the main approaches here. The book is aimed at providing an overall picture of the issues involved in ESD protection circuit design and analysis. It is intended to provide a basis in this field for circuit design and reliability engineers as well as process and device design engineers who have to deal with ESD in integrated circuits.

## 1.2 THE ESD PROBLEM

ESD is the transient discharge of static charge, which can arise from human handling or contact with machines. The mathematics of the generation of static electricity has been presented in some detail in previous works [Bhar83][Greason87]. In a typical work environment, a charge of about 0.6  $\mu\text{C}$  can be induced on a body capacitance of 150 pF, leading to electrostatic potentials of 4000 V or greater. Any contact by the charged human body with a grounded object such as an IC pin can result in a discharge for about 100 ns, with peak currents in the ampere range. The energy associated with this discharge could mean failure to electronic devices and components. Typically, the damage is thermally initiated in the form of device or interconnect burnout. The high currents could also lead to on-chip voltages that are high enough to cause oxide breakdown in thin gate MOS processes. The latter form of damage requires a large amount of energy. Many semiconductor devices can be damaged even at a few hundred volts, but the damage is too weak to be detected easily, resulting in what is known as *walking wounded* or *latency effects* [McAteer82]. A device can be exposed to undetected ESD events, starting in the fabrication area during process [Hill85] and extending through the various manufacturing stages up to the system level. Thus, precautions to suppress ESD become important through all phases of an IC's life.

As mentioned earlier, ESD is a subset of the broad spectrum of EOS, where the EOS family includes lightning and electromagnetic pulses (EMP). EOS, in general, commonly refers to events other than ESD that encompass time scales in the

microsecond and millisecond ranges compared to the 100 ns range associated with ESD. EOS events can occur due to electrical transients at the board level or the system level. They can also occur during device product engineering characterization or during the burn-in test. Although much of the reliability focus has been on ESD, EOS is being increasingly considered to be a major issue demanding more attention as it becomes a significant failure mode in the IC industry. Much of the device physics and analytical modeling discussed here will be equally applicable to EOS stress conditions.

### 1.3 PROTECTING AGAINST ESD

The main ESD problem in a wafer fabrication area is static charge generation, which needs to be suppressed. Prevention methods include the use of antistatic coatings to the materials or the use of air ionizers to neutralize charges. Damage caused by human handling can be reduced by proper use of wrist straps for grounding the accumulated charges and shielded bags for carrying the individual wafers. Static control and awareness are two important programs to combat ESD in the semiconductor-manufacturing environment [McAteer79][Dangelmayer85].

As a second step to reduce ESD effects, protection circuits are implemented within the IC chip [Lindholm85]. With effective protection circuits in place, the packaged device can be handled safely from device characterization to device application. However, the packaging procedure itself can cause serious damage; antistatic precautions are also needed during the wire bonding and assembly phases. Even with good protection circuits, devices are not necessarily immune to ESD once they are on the circuit boards. Other forms of ESD from the charged boards are possible. Thus ESD precautions are important during system assembly as well. Finally, the implementation of effective on-chip protection is a continuous learning experience. Even if not very effective, a relatively weak protection circuit is better than none. A good protection design would be capable of surviving the ESD event and protect the internal transistors connected to the IC pin.

It is a challenging task to design effective protection circuits, and several design iterations can be required to optimize them.

### 1.4 OUTLINE OF THE BOOK

During an ESD event, the on-chip components operate outside their usual range. The behavior of semiconductor circuit elements is not covered by standard texts on semiconductor device physics. A general understanding of this behavior can be obtained from publications on the high current behavior of bipolar devices [Ghandhi77]. Similarly, circuit design and layout for ESD robustness require particular guidelines that have evolved through years of experimental work in this field. The same is true for test methods and characterization. In this book we have

attempted to present coverage of all these aspects, which would enable the reader to gain a broad understanding of ESD in ICs and the main issues involved in improving ESD performance. The book draws from a large publication base in this area, the bulk of which is available through the *Proceedings of the EOS/ESD Symposium*, which is held annually and deals with all areas of ESD. Much of the detailed understanding of ESD in ICs has been presented at this symposium. Brief outlines have been presented in review papers which have presented the state-of-the-art regarding ESD at the time of publication [Amerasekera92][Duvvury93].

The book consists of 12 chapters and an outline of the contents of each chapter is given later. Chapter 2 first presents the details of the ESD phenomena introducing the 'charge' and 'discharge' effects. With this background, Chapter 3 discusses the various appropriate test models and the test methods. These phenomenas are in terms of the voltages, currents, and pulse durations, whereas the test methods are described in terms of the simulations of the events arising from the different stress models. The test methods shown to approximate the phenomena consist of the Human Body Model to represent the human handling, the Machine Model to emulate machine contact, and the Charged Device Model to determine the effects of field-induced charging of the packaged IC. The issues dealing with the accuracy of these models and the commercial testers available to simulate them are also discussed.

To understand the mechanisms of device failures and operation of the semiconductor protection devices under the high current short duration ESD pulses, the device physics behind these will be considered in Chapter 4. The protection device design requires an understanding of the physics involved in resistors, reverse-biased PN diodes, the parasitic *npn* operation of an nMOS transistor, or the latchup operation of a PNP device.

As a new addition to the book, Chapter 5 describes the ESD protection design concepts outlining the general principles used to construct ESD protection circuits and the necessary strategy. This basic background is deemed to be necessary before delving into the protection circuit designs themselves. In Chapter 6, the design requirements for effective protection circuits that can perform without degrading the IC chip functions are discussed. For example, a protection at the input should not affect the gate-oxide reliability, an output protection should have no impact on the output buffer performance, and neither should result in an increase in the leakage current in the chip. The approach taken here will be to demonstrate a synthesis of the protection circuit design needs while considering the optimum design compatible with complex internal IC chip current paths during ESD, or the function of the chip, that is, whether it is floating substrate DRAM or a grounded substrate logic chip. Each individual protection element will first be discussed separately before combining them to form effective protection schemes. Just as important as the protection design is its implementation. The layout of a protection device plays a crucial role in its effectiveness. Both the design and layout techniques are discussed in Chapter 6. As will be demonstrated, effective protection circuit schemes can perform far below the expected

level mainly because of poor implementation. The chapter will focus on the design practices and guidelines for the protection design layouts. Even after an effective design and layout, the full ESD robustness of the IC cannot always be guaranteed.

With the recent advances in technologies, the protection circuit design has become even more challenging. Many of these latest developments are dealt with in Chapter 7. For example, completely new protection concepts had to be introduced to be compatible with high-performance transistors for the deep submicron technologies, or novel concepts had to be developed to accommodate the new IC circuit designs such as mixed-voltage applications and high-voltage applications. The concepts described in this chapter represent the very latest and form the basis for protection strategy across many companies.

To illustrate the transistor phenomena and the design techniques discussed in the earlier chapters, the main failure modes observed in advanced silicon ICs will be discussed in Chapter 8, together with case studies related to the effects of design and layout on ESD performance. This analysis involves a thorough stress methodology for characterization and a full study of the failure modes. Several actual case studies will be presented, which indicate the common, and some times more bizarre, ESD problems. A brief summary of the failure analysis techniques useful for ESD as well as the poststress failure criterion will be reviewed.

The development of newer protection techniques are needed because of the degradation of the existing protection devices with advances in process technologies as shown in Figure 1.2. In many cases, process dependence of ESD performance can frustrate any attempts to achieve the specified ESD levels for the product. Chapter 9 discusses the principal aspects related to process effects, such as the impact of LDD junctions or silicided diffusions on ESD performance. The specifics of the process effects and methods to monitor these process effects will be reviewed.

In Chapter 10, a review of the device modeling techniques based on the high current behavior of the protection circuits is given. These look at the approaches used in analytical and numerical modeling of the ESD phenomena in semiconductor devices. This continues to be an evolving field and a lot of work is currently being done to uncover the underlying mechanisms involved and identify the main predictive indicators to be used. The eventual goal is the capability to develop and evaluate high-performance ESD protection circuits in new processes using simulation techniques.

To enable more specifically the design of ESD protection circuits, there have been some recent advances in simulation methods. Chapter 11 is a new addition which gives details of circuit simulations that can be used for protection circuit development as well as in the analysis of the protection circuit behavior under ESD conditions. The latter capacity is increasingly becoming important as demand grows for efficient protection designs with minimum iterations in silicon. The eventual goal is to achieve first pass success which is within reach with the methods described in Chapters 10 and 11.

Finally, in Chapter 12 a summary of the main issues is given, together with an evaluation of the state-of-the-art with regard to protection techniques and future ESD requirements and directions for further work in this area.

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