

## PREFACE

This book provides the detailed information on power distribution network design in integrated circuit chips. Power distribution network design is a critical part of the job in circuit design and physical integration for high-speed chips.

The  $IR$  drop and  $di/dt$  noise associated with the power distribution networks are crucial to circuit timing and performance. Due to the complexity of the millions of gates and interconnects in modern VLSI chips, power network analysis is accomplished using CAD tools. These tools take the layout database, usually in GDSII files, extract the RC parasitic for the power distribution network, and model the current consumption for switching devices.

A fast circuit simulation is done for the electrical model of the power distribution network in order to determine the  $IR$  drop or other supply voltage noises, as well as the current density of metal power lines for checking electromigration failures.

In addition, the decoupling capacitors are inserted into the power network for stabilizing the supply voltages in local regions where current surges occur from time to time due to clock and logic operations. The decoupling capacitors and power distribution networks are required in some optimal form not only on-chip, but also on the package and at system levels.

This book will explain the design issues, guidelines, examples,

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and CAD tools for the power distribution of the VLSI chip and package. The user guide of the VoltageStorm™ tool from Cadence Design Systems, Inc. is referred to throughout [51], together with the author's experience using this tool in designs.

The book is organized into seven chapters. Chapter 1 is an introduction to the power supply network, power network modeling, decoupling capacitors, and process scaling trends. Chapter 2 illustrates the design perspectives for the power distribution network, including power network planning, layout specifications, decoupling capacitance insertion, modeling and analysis of power networks, and *IR* drop analysis and reduction. Chapter 3 explores electromigration phenomena for the on-chip power distribution network.

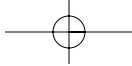
Chapter 4 discusses *IR* drop analysis methodology. It is taken primarily from the VoltageStorm™ tool, using both static and dynamic analysis methods. The static method is performed for some level worst-case *IR* drop analysis without the knowledge of input vectors at the chip's primary inputs. Chapter 5 describes the commands and user interfaces of the VoltageStorm™ tool from Cadence Design Systems, Inc. [51]. Chapter 6 lists the microprocessor design examples, with a focus on on-chip power distribution. Readers will gain the insights into industry chip design for power distribution networks from these examples.

Chapter 7 discusses the flip-chip and package design issues, since the package is a part of the global power distribution. A case study has been provided in this chapter for selecting the package options, based on the performance requirements for the power supply. Power network measurement techniques from silicon are also discussed at the end of Chapter 7.

A glossary of key words and basic terms is provided at the end of the book to help understand the basic concepts in VLSI design and power distribution.

With the continually decreasing supply voltages and the increasing transistor switching currents on-chip, power supply noises on-chip remains the challenging issue for high-performance chip design. More and more research will be needed in the future in CAD tools for switching current modeling and accurate power network analysis. The design methodology for power delivery will need to consider the performance, layout area, and package technology optimization for future chips.

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